

Scope

This application note is a guide to implement ISO compliant communications with the MLX90121 RFID transceiver. The users of the MLX90121 will be taught on how to transmit symbols and how to synchronize the circuit (usage of the LTC, majority voting functions). Several ISO communication examples will be described in detail.

Glossary of Terms

RFID	Radio Frequency IDentification
ISO	International Organization for Standardization / International Electro-technical Commission .
NRZ	Non Return to Zero
ASK, FSK, PSK	Amplitude, Frequency, Phase Shift Keying

Transmission

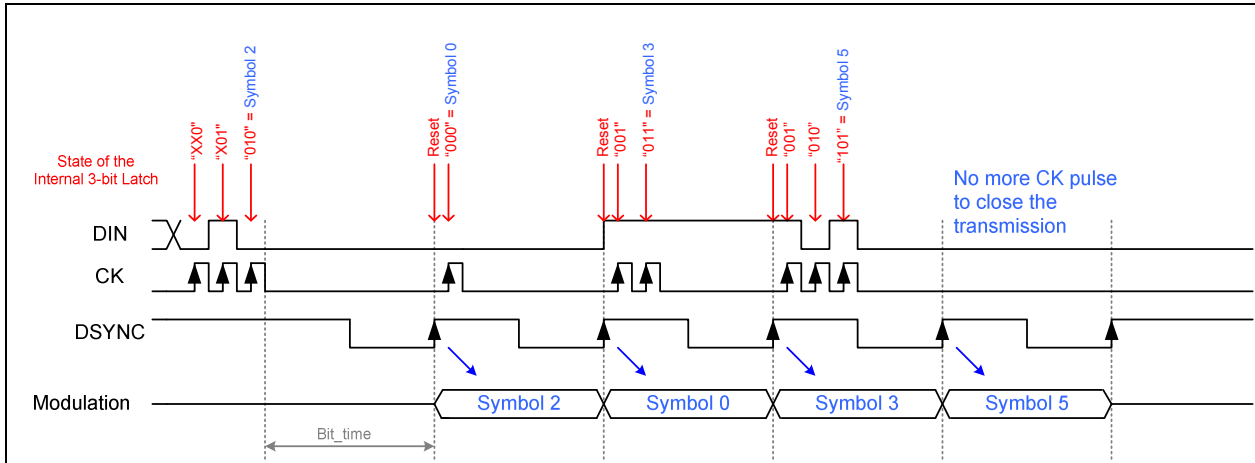
Programmable symbol encoder

The MLX90121 has been designed with an internal programmable encoder which allows pre-defining six symbols. After configuration, symbols can be sent by simply specifying their address, using the pins CK and DIN. The corresponding address is internally stored in a 3-bit latch. In order to start the transmission three CK pulses are needed to specify the address of the first symbol. During the transmission, it is not necessary to always specify the 3 bits of address because the internal latch is reset to "000" each time the encoder starts to send a symbol. Therefore, the symbols zero and one can be specified with only one CK pulse (all other bits will remain to 0), the symbols two and three with two CK pulses and the symbols four, five and six with three CK pulses.

By this way, the load of the microcontroller can be optimized if symbols which are currently used are predefined with a low address (e.g. address 0 and 1 are used for ISO14443).

The MLX90121 provides a synchronization signal DSYNC which informs the external microcontroller that the programmed symbol is being sent (rising edge). The time between two successive rising edges of DSYNC depends on the symbol length pre-programmed in the register *EncTimeRef*.

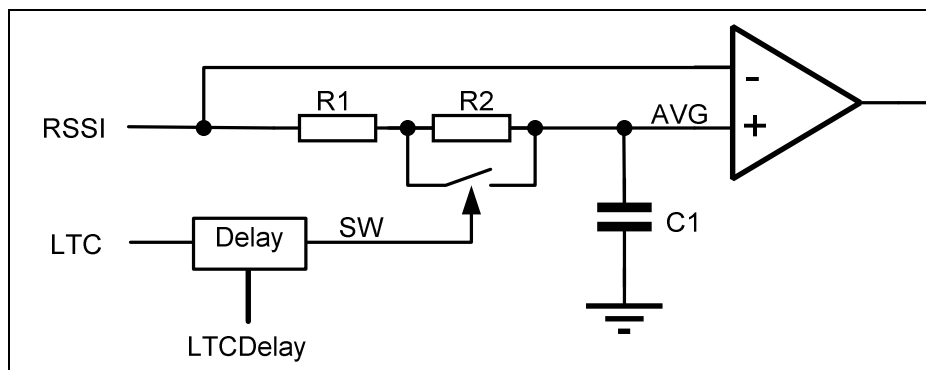
The transmission is terminated when no more CK pulses are sent after the last symbol transmitted.



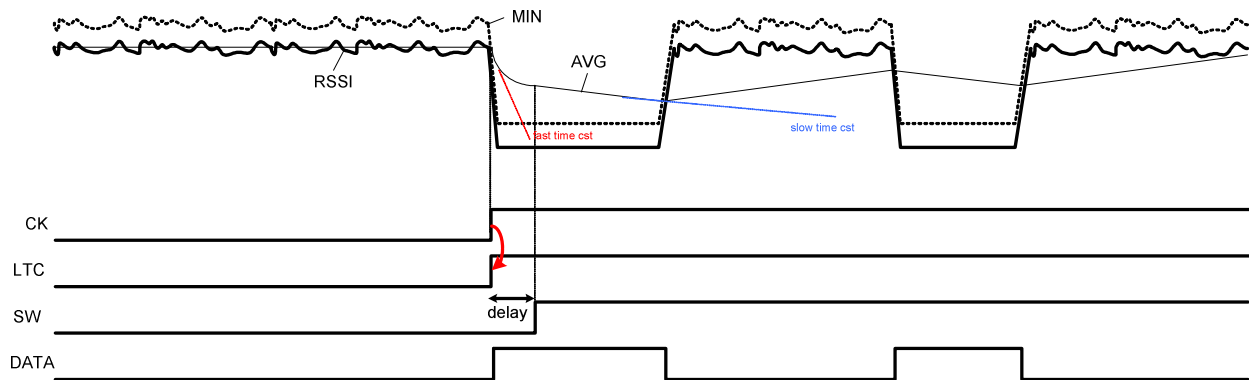
Reception

ASK decoding

As already explained in the datasheet of the MLX90121, a data slicer is used to digitalize the ASK information coming from the analog chain (RSSI).



The internal signal LTC (Low Time Constant) controls the time constant of the data slicer. It is used at the beginning of the response to switch between a fast and a slow time constant as shown in the drawing below.



Some delay must be added before switching from fast to slow time constant to ensure the AVG signal reaches an appropriate medium level to get the maximum of sensitivity. This delay will be adjusted according to the standard used. For more information, please refer to the ISO register's configuration proposed in the datasheet of the MLX90121.

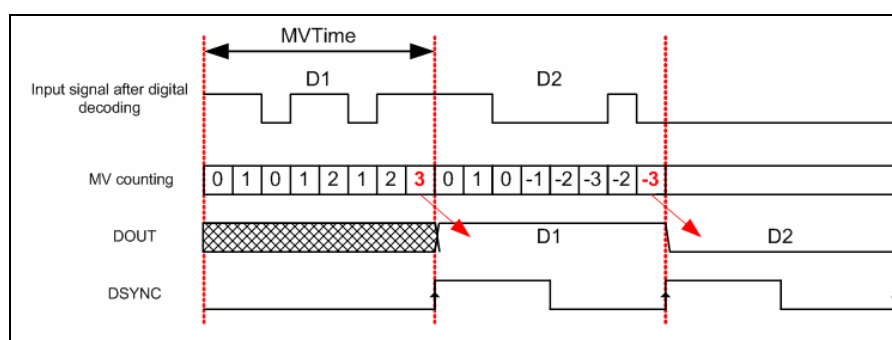
The internal signal LTC is started by asserting high the CK pin. **Therefore, to receive correct ASK information, the application (microcontroller) needs to assert the CK pin at the beginning of the reception frame (transponder's reply).**

Majority voting (MV)

The MV is up and down counter (logical '1' = count up, logical '0' = count down) which samples the digital information during a predefined time interval configured in the register *DecTimeRef*. At the end of the time interval, the MV block takes the decision of the level of the signal according to the counting result X:

$X > \text{zero} \Rightarrow \text{logical '1'}$.
 $X \leq \text{zero} \Rightarrow \text{logical '0'}$.

The result is then provided by the MLX90121 on the DOUT pin with a synchronization signal DSYNC that can be used by the external microcontroller. Data on the pin DOUT will be delayed of MVTime from the real antenna modulation.



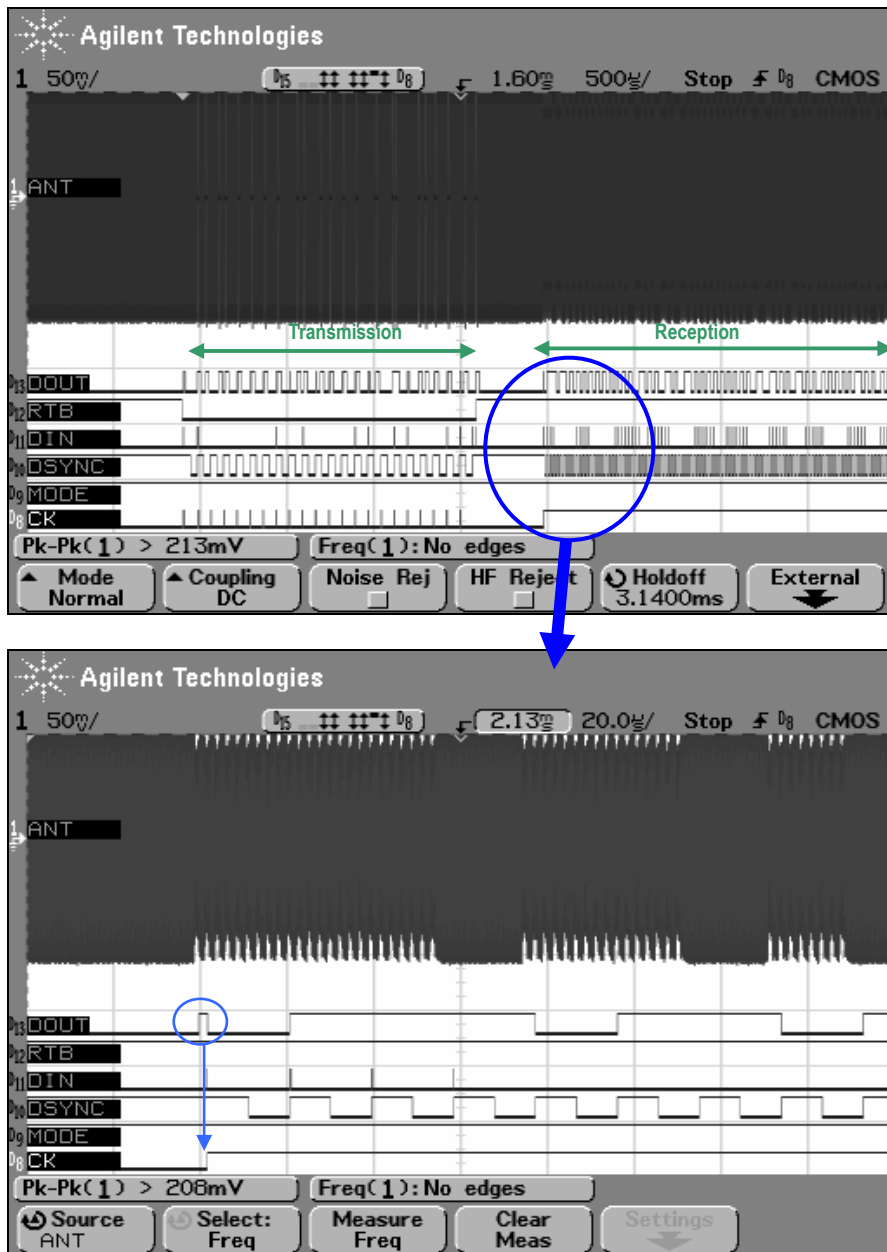
The MV block is time related and must be started by the application (external microcontroller) by asserting high the CK pin at the beginning of the reception frame (transponder's reply).

Conclusion

As explained above, for the ASK reception, the CK pin of the MLX90121 must be asserted high at the beginning of the reception frame. Moreover, Melexis highly recommend to use the with the majority voting block for the reception, which will be started by using the same method. **Therefore, to perform an ISO communication, the CK pin of the MLX90121 must be asserted high at the beginning of the reception frame, this whatever the type of decoding used.**

Synchronization

After sending the request, the application (external microcontroller) must look at the **DOUT** pin to find the beginning of the transponder's reply to start the MV and the data slicer (if ASK decoder is used). This is done by asserting high the **CK** pin. The synchronization of the MLX90121 is illustrated with the pictures below.

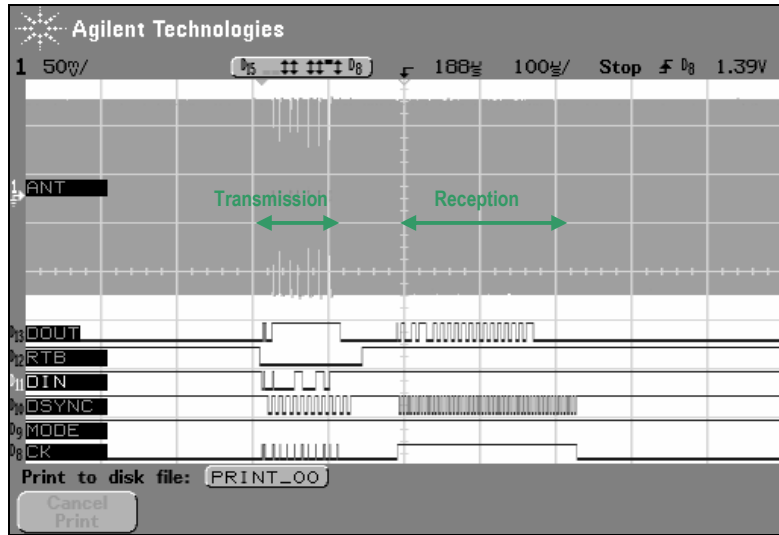


The signal CK is raised up as soon as a rising edge on the DOUT pin is detected by the microcontroller. As there is no automatic recognition in the MLX90121, the external microcontroller needs to poll the pin DOUT to detect this rising edge.

Examples

ISO14443 type A

The pictures below show a complete communication performed in ISO14443 A (command REQA). The digital registers of the MLX90121 are configured according to the register's configuration defined in the chapter 13 of the MLX90121 datasheet.

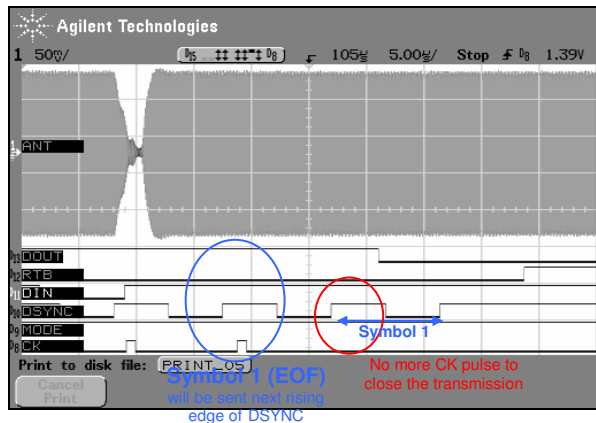
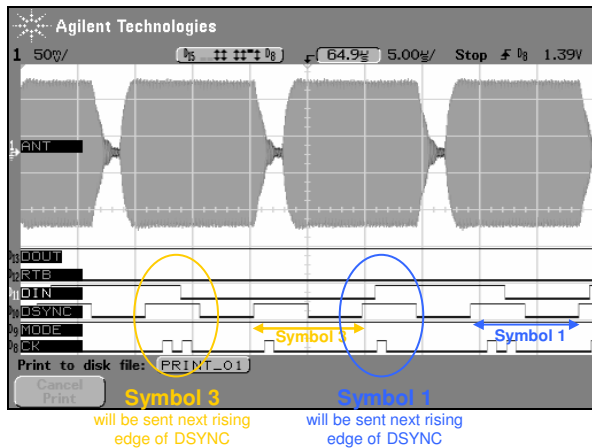


Symbol transmission

As shown below, three symbols are used to communicate in ISO14443 A. Each of them will be programmed with a time length of $1/106\text{kbaud} = 9,44\mu\text{s}$ (EncoderTimeRef = 0x03).

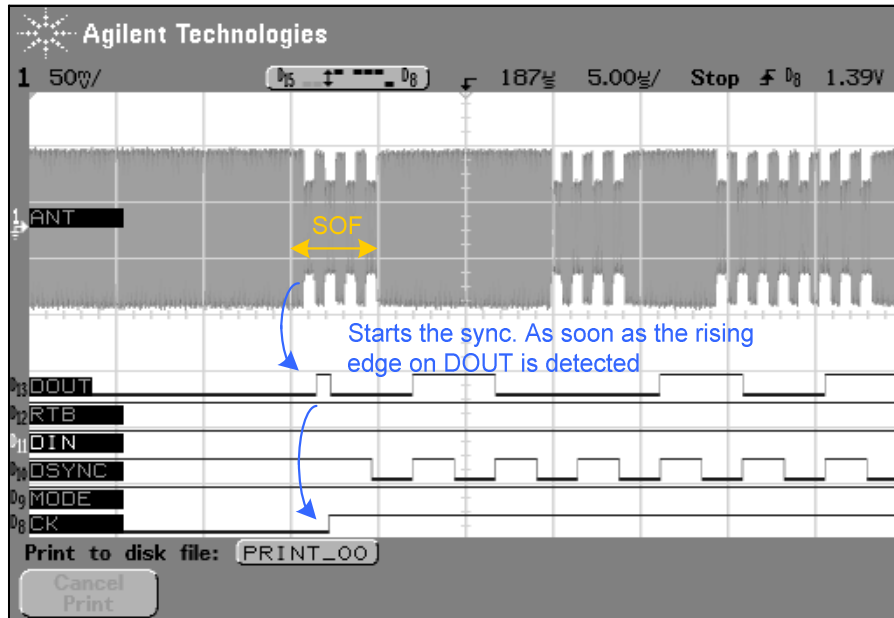
ISO14443-A		
Symbol	Name	Code
Sym0	X	11110011
Sym1	Y	11111111
Sym2	Z	00111111

The following pictures are a zoom to show in detail the transmission of the symbols.



Reception

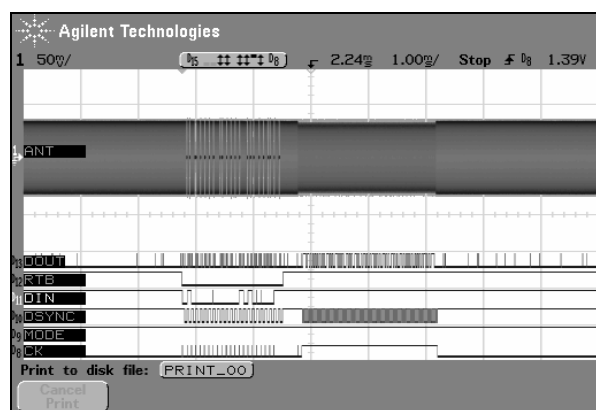
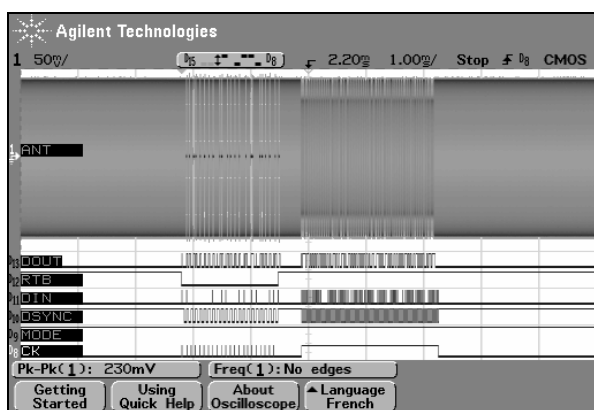
For all inventory commands (level 3 of the ISO14443 standard) the transponder replies with a specified time between 86 and 91µs. Therefore, the microcontroller can easily detect the rising edge on DOUT to start the synchronization, as shown below.



Note: For several commands defined in the level 4 of the ISO14443 standard, the time between the request and the response is not fixed and can vary from 86µs to 5s. Therefore, a more complex procedure must be implemented to avoid synchronizing on a noise (e.g glitch filter).

ISO15693 single and dual sub-carrier

The pictures below show a complete communication performed in ISO15693 single and dual sub-carrier, 100% (Read Single Block command, 1 out of 4). The digital registers of the MLX90121 are configured according to the register's configuration defined in the chapter 13 of the MLX90121 datasheet.



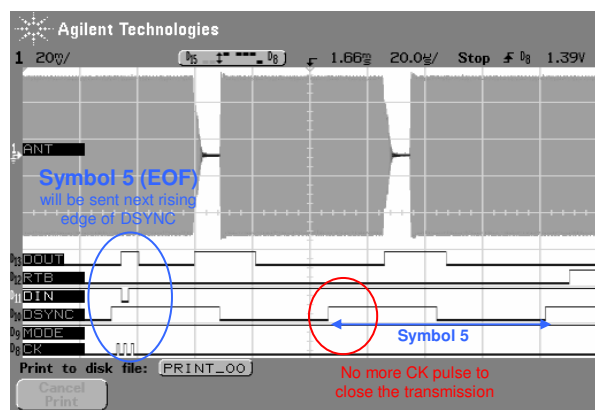
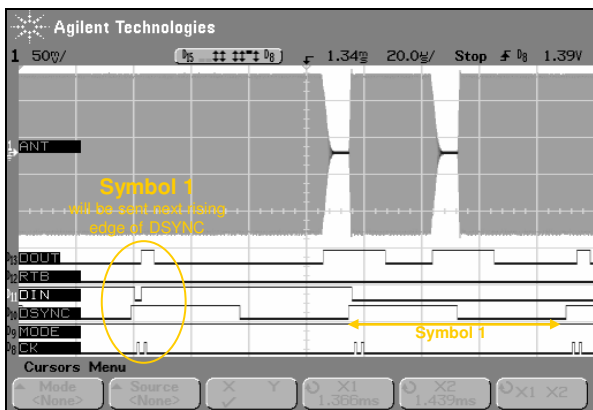
Symbol transmission

As shown below, five symbols are used to communicate in ISO15693. Each of them will be programmed with a time length of $2/(2*26,5\text{kBaud}) = 75,52\mu\text{s}$ (EncoderTimeRef = 0x1F).

ISO15693 (1 out of 4)		
Symbol	Name	Code
Sym0	Pulse1	10111111
Sym1	Pulse2	11101111
Sym2	Pulse3	11111011

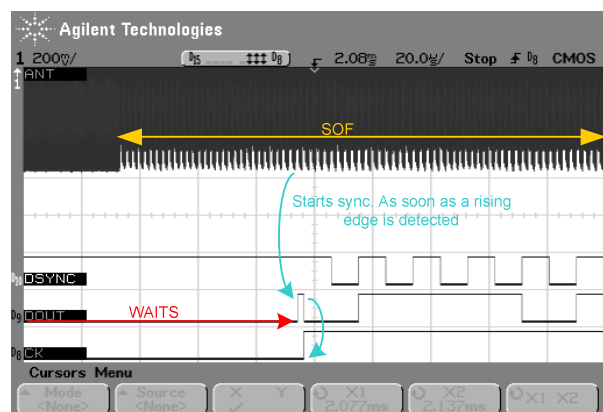
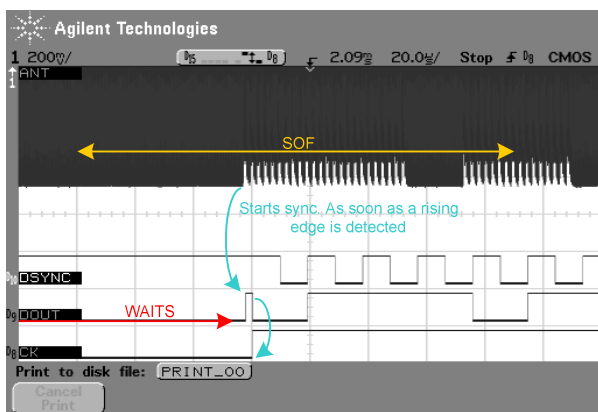
ISO15693 (1 out of 4)		
Symbol	Name	Code
Sym3	Pulse4	11111110
Sym4	SOF	01111011
Sym5	EOF	11011111

The following pictures are a zoom to show in detail the symbol transmission for both ISO15693 standards.



Reception

In the standard ISO15693 single and dual sub-carrier, the transponder will always reply at a fixed time after receiving the request from the transceiver ($312\mu\text{s} \pm 2\mu\text{s}$). Therefore, the external microcontroller will poll the pin DOUT just before the transponder's reply to avoid bad synchronization on noise (parasitic glitch mainly in FSK reception). The following pictures illustrate the synchronization procedure for ISO15693 single and dual sub-carrier.

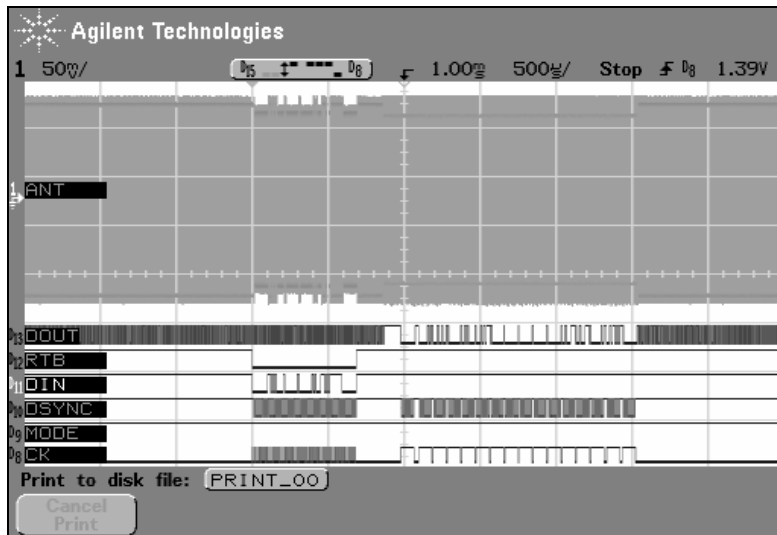


The microcontroller waits for a time of about $364\mu\text{s}$ to avoid a bad synchronization on a parasitic glitch. After this time, the microcontroller polls DOUT and starts the synchronization as soon as a rising edge is detected.

Note: For the commands "write single block" and "write multiple blocks", more time are needed by the transponder to write its EEPROM memory, an option flag can be set to force the transponder to reply after reader's request (slots). Therefore, the synchronization can be done exactly as explained above.

ISO14443 type B

The pictures below show a complete communication performed in ISO14443 B (command REQB). The digital registers of the MLX90121 are configured according to the register's configuration defined in the chapter 13 of the MLX90121 datasheet.

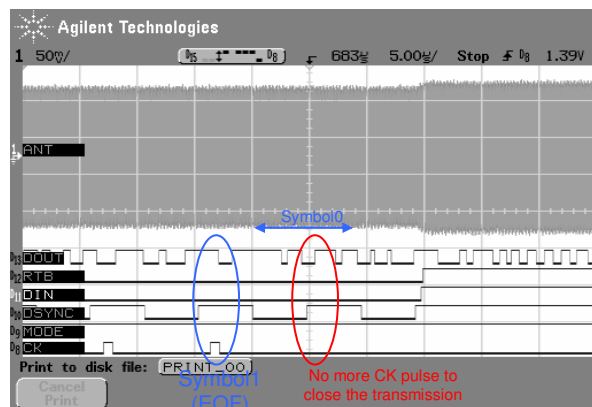
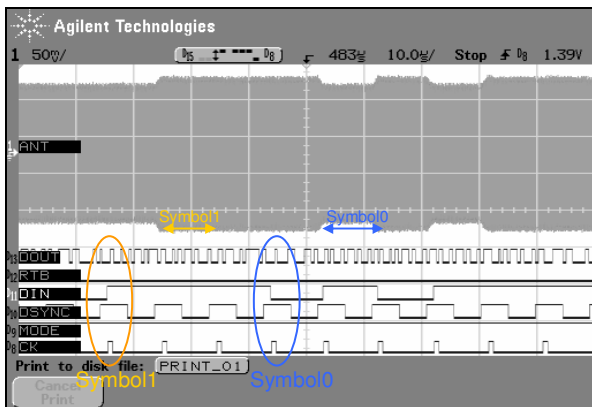


Symbol transmission

Data in ISO14443B are encoded in NRZ. Therefore, only the symbols '0' and '1' are used to communicate with a time length of $1/106\text{kbaud} = 9,44\mu\text{s}$ (register EncoderTimeRef = 0x03).

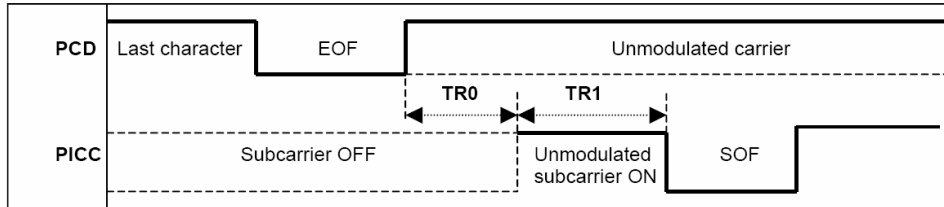
ISO14443-B		
Symbol	Name	Code
Sym0	L	00000000
Sym1	H	11111111

The following pictures show in detail the symbol transmission for ISO14443B standard.

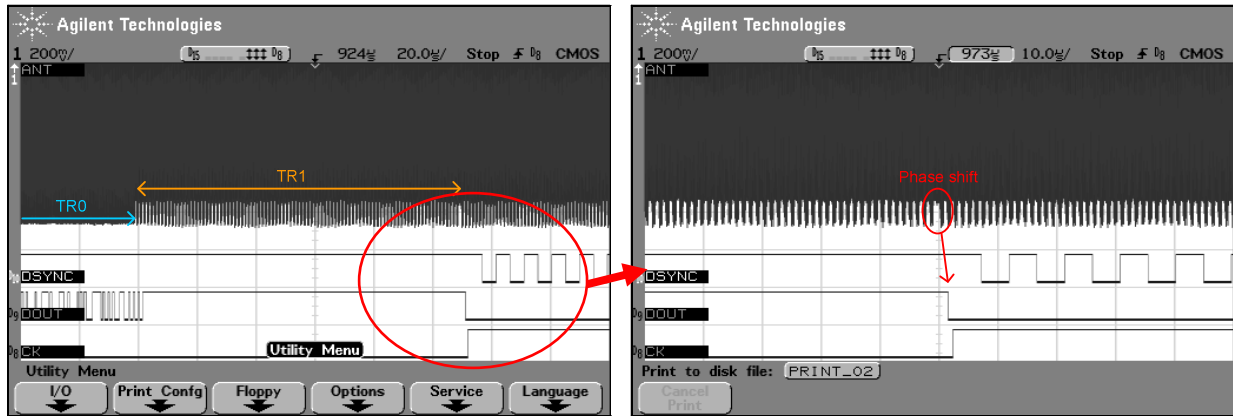


Reception

The standard ISO14443 B has been specified with a long synchronization times TR0 and TR1, as shown in the following diagram.



The time TR1 will be used by the microcontroller to detect the beginning of the response and to rise up the pin CK. The pictures above illustrate the synchronization procedure for the ISO14443 type B.

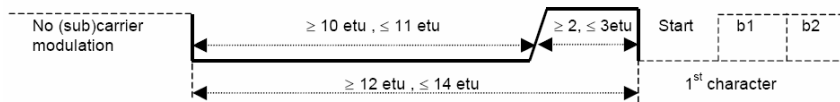


As shown in the pictures above, when the transponder starts to modulate, the noise on the pin DOUT stops. Therefore, it is easy for the microcontroller to find the time TR1, during which the transponder sends the un-modulated sub-carrier, and to start the MV directly after the detection of the first phase shift (transition on DOUT). One should keep in mind that the polarity of the signal DOUT can be inverted when the PSK decoder is used.

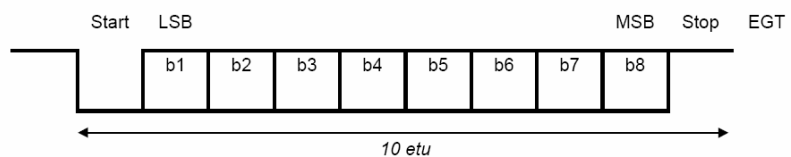
EGT (Extra Guard Time)

The standard ISO14443 type B allows a transponder to reply using a SOF or an EGT with a non integer number of bit (ETU, elementary time unit). For more information, please refer to the standard specification ISO14443-3.

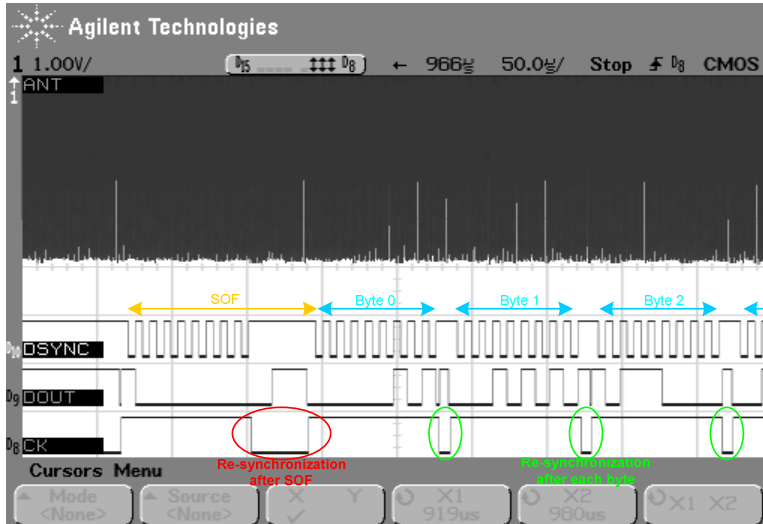
Start of Frame SOF:



Extra Guard Time
EGT between bytes:

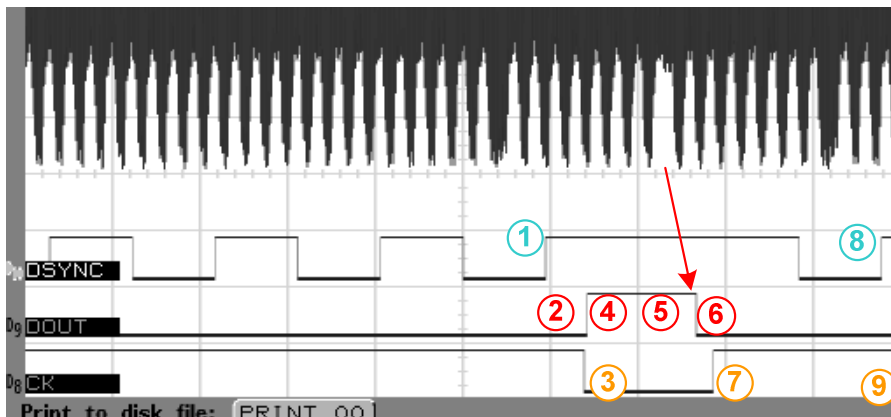


This will be a problem for the MLX90121 as the MV block is synchronized on the incoming stream. The following procedure must be implemented in the microcontroller to re-synchronize to MLX90121 on the response of the transponder after each byte received including the SOF.



The idea is to restart the synchronization after the SOF and between each character. After the last data bit is received, CK signal is reset and the stop bit is polled by the microcontroller. When the start bit is received, CK is asserted high and the next character is decoded. The same procedure is implemented after the detection of the SOF.

The following picture shows the synchronization after the reception of the first byte.



On the rising edge of DSYNC (1) the last data bit is read (2). Then CK is asserted low (3) to disable the MV. DOUT is now the decoded signal without the majority voting function (4). The stop bit is polled by the microcontroller on DOUT (5) until it switches (6). CK is immediately set (7). At the rising edge (8) of DSYNC, the next bit can be read on DOUT (9). This is the start bit of the next character.