

TH7122 and TH71221 Used In Narrow Band FSK Applications

1 Narrow band considerations

The most common application for low power transceivers is in applications where the channel bandwidth and spacing are relatively wide. In these cases, the peak FSK deviation is usually around 25 to 50kHz, and the channel spacing is usually 200kHz or more. In the case of the TH7122x, the intermediate frequency (IF) filter is usually a low cost FM receiver filter with a bandwidth from 150 to 250kHz. For these applications the VCO noise is usually not a big consideration because the frequency deviation causes a voltage swing at the demodulator output which is much greater than the noise. Also, the loop bandwidth is usually wide because the reference frequency is high. This allows for modulation of the reference frequency by simple switching of the load capacitance on a crystal.

The TH7122x is designed to work in these applications and gives very good results. However, if it is used in narrow band applications with small channel spacing such as 12.5 or 25kHz, the loop bandwidth must be small to allow for stable PLL operation and to suppress the reference spurs sufficiently. The reference frequency for the integer N synthesizer is equal to the channel spacing. For these designs, the VCO noise becomes very important and some changes need to be made to the usual application circuit to improve the performance.

A second consideration in narrow band applications is that the transmitter which uses the same PLL as the receiver must be capable of FSK generation. Since the PLL bandwidth must be narrow, it is necessary to generate FSK by modulating the VCO outside the loop bandwidth. If FSK modulation down to DC is required, it is also necessary to modulate the reference crystal oscillator at the low frequencies and the VCO at high frequencies. This is often referred to as two point modulation. The difficult part is to make a smooth transition from modulation of the VCO to modulation of the reference. In this application, we will assume DC modulation is not needed and so the low loop frequency can be set to accommodate the widest data pulses.

2 VCO design

In order to reduce the phase noise of the VCO in the TH7122x, the impedance of the tuned circuit must be reduced. The negative resistance oscillator goes into saturation with high impedance load and reduces the Q of the resonator. The resonator Q is reduced further by the relatively low Q of the internal varactor diode. In the usual application, the inductance of the tuned circuit is determined by the capacitance of the internal varactor and any fixed capacitance across the VCO tank coil. The capacitance in parallel with the coil can be increased, but this limits the tuning range which must be large enough to tune the offset between the transmit frequency and VCO frequency for receive. Note the offset frequency corresponds to the IF because the TH7122x constitutes a super-heterodyne receiver. Usually, the IF is 10.7MHz. The solution is to use a small inductance together with an external varactor but not to make the tuned circuit impedance smaller.

Fig. 3 shows the circuit of an evaluation board with a small tuning inductor and an external varactor to increase the tuning capacitance. In this case a BB639 diode was used because it was available and is a low cost diode usually used for TV tuners. Almost any tuning diode with enough capacitance could be used by simply adjusting C0. Care must be taken not to make L0 so small that the oscillator does not oscillate. Since the oscillator current is programmable, the oscillator can be checked for operation at the lowest current setting and then operated at the highest current for lowest noise.

3 PLL setup

In order to design the PLL loop filter, it is first necessary to know the phase detector constant and VCO tuning sensitivity K_{VCO} around the desired frequency. There are two ways to determine K_{VCO} :

1. Tune the VCO with a variable voltage from a potentiometer (e.g. 1k Ω) or power supply and measure the output frequency with a counter or spectrum analyzer. This can be done by simply connecting the variable voltage via a 100k Ω resistor to pin 23 of the TH7122x. Using the software for programming the TH7122x with a personal computer, set it to transmit mode, VCOCUR to '11' high current2, and PACTRL to '1' so the PA is always on. Adjust the tuning voltage and measure the output frequency.

2. Set-up the TH7122x to operate at the desired frequency in transmit mode using the loop filter on the evaluation board. Connect a high-impedance digital voltmeter to pin 23, the charge pump output. Using the TH7122x software, set the transmitter to frequencies around the operating frequency, and measure the tuning voltage at each frequency. Be careful to keep capacitive and resistive loading at pin 23 should be as low as possible to avoid influencing the over-all stability of the PLL.

A tuning curve taken on an evaluation board is shown in **Fig. 1**. In this example it can be seen that the slope of the tuning voltage around 434MHz is typically about 14MHz/Volt. Expressed in an angular relation the K_{VCO} yields in

$$K_{VCO} = 2\pi \cdot 13 \frac{\text{MHz}}{\text{V}} = 81.7 \cdot 10^6 \frac{\text{rad}}{\text{s}} \frac{1}{\text{V}}.$$

A second design parameter is the gain of the phase detector K_{PD} . This parameter is proportional to the charge pump current I_{CP} which is 260 μ A by default. The phase detector constant is expressed as

$$K_{PD} = \frac{I_{CP}}{2\pi} = 41.4 \frac{\mu\text{A}}{\text{rad}}.$$

As we will see below the 2π term cancels out since K_{PD} and K_{VCO} are always multiplied together.

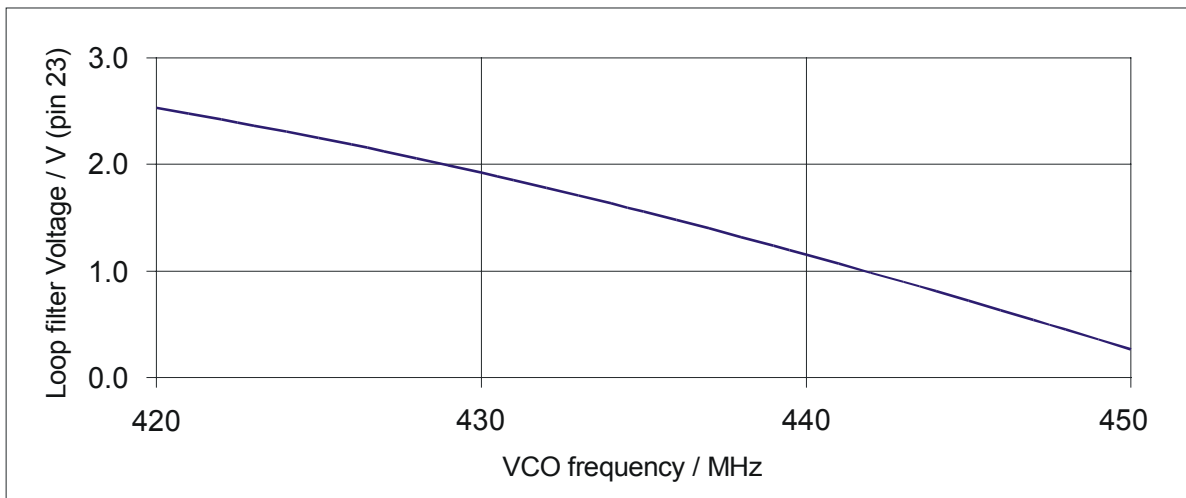


Fig. 1: TH7122x VCO tuning curve for 434MHz center frequency

The recommended loop filter topology is a 2nd order as depicted in **Fig. 2**. From the filter transfer function $F(s)$ we can obtain a zero and a non-DC pole frequency¹:

$$\omega_z = \frac{1}{R_F \cdot C_{F1}} \qquad \omega_p = \frac{C_{F1} + C_{F2}}{C_{F1} \cdot C_{F2} \cdot R_F}$$

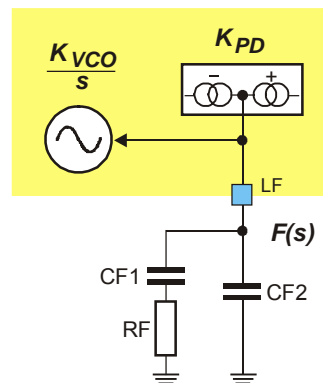
¹ Investigation of the details of the PLL behaviour would require more space than this application note allows. A more detailed analysis of the PLL behaviour can be found in references [1] – [3].

The 3dB bandwidth of the PLL in a closed loop configuration is approximately the transit frequency ω_T of the loop filter. Since C_{F2} is much smaller than C_{F1} in most of the cases, ω_T can be approximated as described in [4]:

$$\omega_T \approx \frac{K_{PD} \cdot K_{VCO} \cdot R_F}{N} \cdot \frac{C_{F1}}{C_{F1} + C_{F2}} \approx \frac{K_{PD} \cdot K_{VCO} \cdot R_F}{N}$$

In these equations N represents the value of the feedback divider. For a stable loop the available phase margin is of importance. It should be in between 30 and 70 degrees. To ensure enough phase margin at the transit frequency ω_T , the zero frequency should be located M times below and the pole frequency M times above ω_T . As mentioned in [4] a factor M of four gives a phase margin of approximately 60 degrees. With M = 2.5 the phase margin will be approximately 45 degrees.

Fig. 2: 2nd order Loop filter



By using these equations the loop-filter elements can be easily obtained:

$$R_F = \frac{N}{K_{PD} \cdot K_{VCO}} \cdot \omega_T$$

$$C_{F1} = \frac{M}{R_F \cdot \omega_T}$$

$$C_{F2} = \frac{1}{M \cdot R_F \cdot \omega_T}$$

This approximation is quite accurate for calculating the loop filter elements. Normally the step size between the available component values is larger than the error using this calculation method, so that there is no need to use the more complex exact formulas. Nevertheless the exact calculation can be found in [1-3].

Example: If a channel step size of 12.5kHz is used, a feedback divider of N = 34720 is necessary to achieve a desired operating frequency of 434MHz. Assume a narrow loop frequency, ω_T of about $2\pi \cdot 50$ Hz because of the external VCO modulation. In case of direct modulation of the VCO as a rule of thumb the lowest data signal frequency should be 10 times higher than the loop frequency. To insure loop stability we want a phase margin of about 45 degrees, so the factor M is 2.5. With the equations above and the calculated gains K_{PD} and K_{VCO} the loop filter elements result in:

$$C_{F1} = 2.2 \mu\text{F} \quad C_{F2} = 470 \text{ nF} \quad R_F = 3.3 \text{ k}\Omega$$

The complete narrow band transceiver application schematic is show in **Fig. 3**

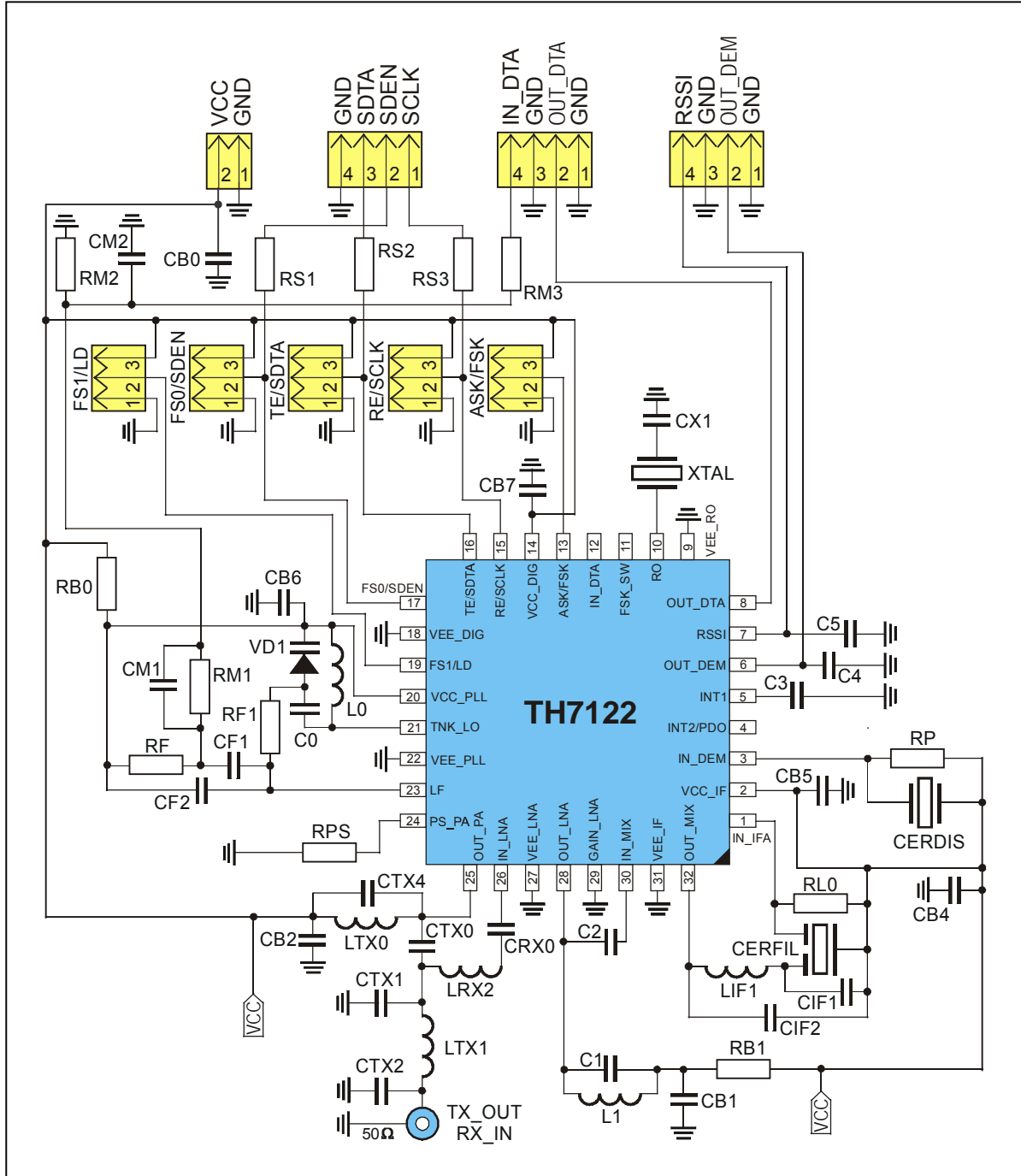


Fig. 3: TH7122x circuit schematic for narrow band applications

4 Transmitter Set-Up

Continuing our example from the previous section, assume we want a peak FSK deviation of 2.5kHz with a 3.0V logic signal. Since the slope of the VCO control voltage is 13MHz/V, this would require a level of 192uV. If we make $R_{M1} = 1M\Omega$, then the input to it would be 58mV. For the FSK modulation to have flat frequency response, the time constant of $R_{M1} \cdot C_{M1}$ should match the time constant of $C_{F2} \cdot R_F$, so $C_{M1} = 1.5nF$. Additional attenuation is needed so done by adding R_{M2} and R_{M3} to the data input connector.

The modulation bandwidth of the VCO is very wide when the loop is modulated, so it may be desirable to shape the data signal in order to limit the occupied bandwidth of the RF signal. This has been done by adding C_{M2} across the input attenuator.

Fig. 4 and **Fig. 5** show the RF output signal in CW mode and with modulation applied to the IN_DTA pin, respectively.

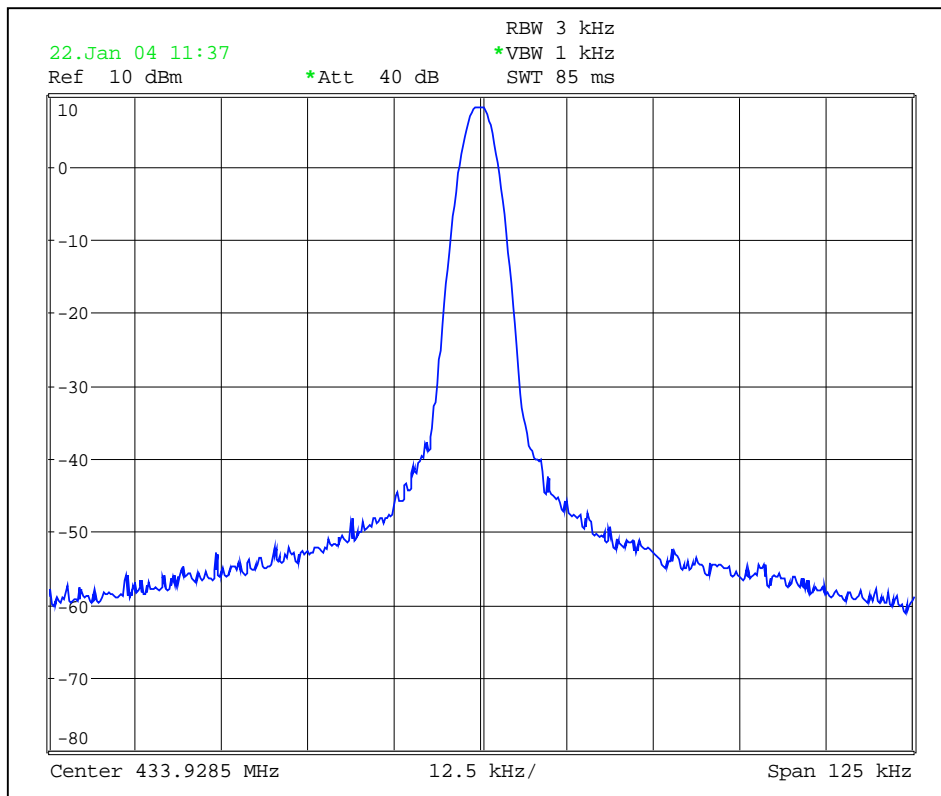


Fig. 4: CW output spectrum of the TH7122x in transmit mode

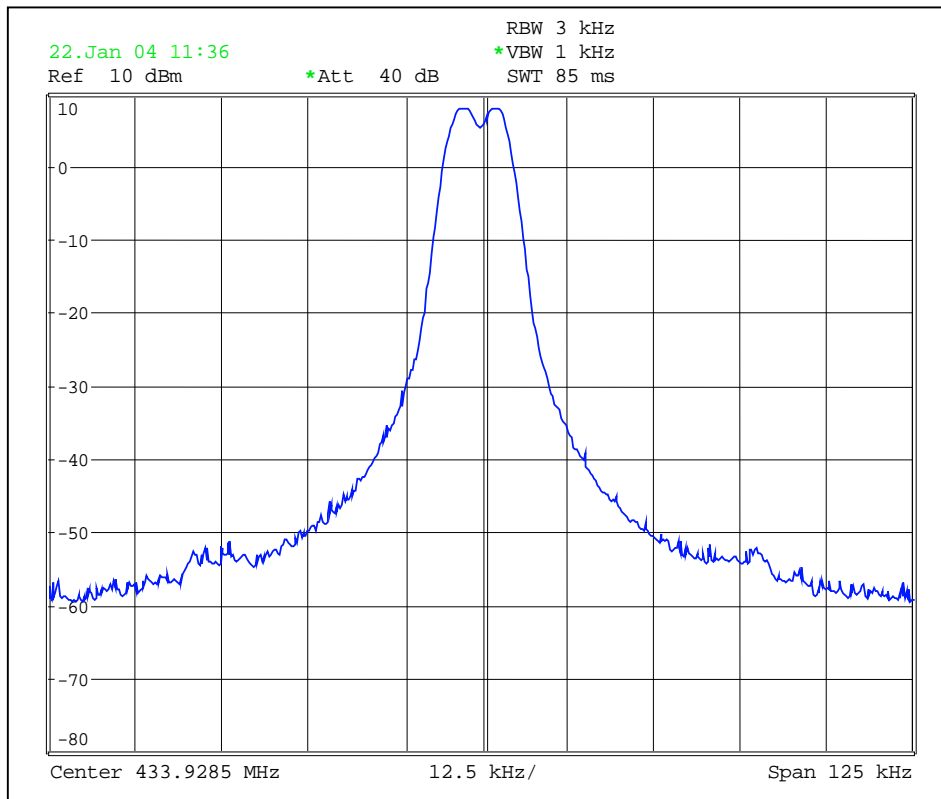


Fig. 5: FSK modulation spectrum of the TH7122x in transmit mode

5 Receiver

The receiver part of the TH7122x application circuit as shown in **Fig. 3** contains a ceramic filter with a 20kHz bandwidth. LIF1, CIF1 and CIF2 are used to match the 330Ω output impedance to the required 600Ω of the ceramic filter. Additionally this circuitry reduces out-of-band spurious responses. RL0 in parallel to the input impedance of the IF amplifier is used to load the filter as specified. The 20dB bandwidth of this filter is approx. 95kHz.

In systems with 12.5kHz channel spacing, the required channel selectivity is higher. This can be achieved by connecting two filters in cascade as shown in **Fig. 6**. In this case, a 4-pole 10.7MHz crystal filter is shown. This is usually made up of a cascade of two 2-pole filters (FIL1 and FIL2). The series inductor between the mixer output and FIL1 as well as capacitor in parallel to the filter input match the mixer output impedance to the 1.8kΩ impedance required by the filter. The input resistance of the IF amplifier is approximately 2kΩ, so this is close enough to the required filter load. The maximum stop-band attenuation of this filter is about 40dB which is about the maximum which can be obtained because of leakage between pins 1 and 32 of the TH7122x.

If more selectivity is desired, a dual conversion arrangement with an external mixer should be considered. However, the maximum selectivity will be limited by the VCO noise in the adjacent channel. The maximum signal-to-noise ratio is also determined by the VCO noise. In this receiver, with a peak FM deviation of 2.5kHz, it is about 36dB. This was measured over the frequency range from 20Hz to 20kHz.

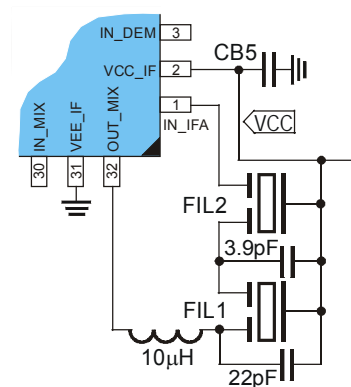


Fig. 6 Cascaded filter configuration

5.1 Component Values for Fig. 3

Part	Size	Value @ 434 MHz	Tolerance	Description
C0	0603	8.2 pF	±5%	VCO tank capacitor
C1	0603	4.7 pF	±5%	LNA output tank capacitor
C2	0603	1.5 pF	±5%	MIX input matching capacitor
C3	0805	10 nF	±10%	data slicer capacitor
C4	0805	1 nF	±10%	demodulator output low-pass capacitor
C5	0805	1.5 nF	±10%	RSSI output low-pass capacitor
CB0	1210	10 μF	±10%	de-coupling capacitor
CB1	0603	330 pF	±10%	de-coupling capacitor
CB2	0805	330 pF	±10%	de-coupling capacitor
CB4	0603	10 nF	±10%	de-coupling capacitor
CB5	0603	100 nF	±10%	de-coupling capacitor
CB6	0603	100 pF	±10%	de-coupling capacitor
CB7	0603	100 nF	±10%	de-coupling capacitor
CF1	0603	1.0 μF	±5%	loop filter capacitor
CF2	0805	100 nF	±10%	loop filter capacitor
CIF1	0603	180 pF	±5%	filter matching capacitor
CIF2	0603	220 pF	±5%	filter matching capacitor
CM1	0603	560 pF	±5%	modulation capacitor
CM2	0603	10 nF	±10%	modulation capacitor
CX1	0805	47 pF	±5%	RO capacitor
CRX0	0603	100 pF	±5%	RX coupling capacitor
CTX0	0603	100 pF	±5%	TX coupling capacitor
CTX1	0805	5.6 pF	±5%	TX impedance matching capacitor
CTX2	0805	4.7 pF	±5%	TX impedance matching capacitor
CTX4	0603	4.7 pF	±5%	TX impedance matching capacitor
RB0, RB1	0603	100 Ω	±5%	protection resistor
RF	0603	5.6 kΩ	±5%	loop filter resistor
RF1	0603	10 kΩ	±5%	varactor bias resistor
RL0	0603	820 Ω	±5%	CERFIL loading, optionally
RM1	0603	1 MΩ	±5%	modulation resistor
RM2	0603	390 Ω	±5%	modulation resistor
RM3	0603	10 kΩ	±5%	modulation resistor
RP	0603	4.7 kΩ	±5%	CERRES loading resistor
RPS	0603	33 kΩ	±5%	power-select resistor
RS1 to RS3	0603	10 kΩ	±5%	protection resistor
LIF1	0603	2.2 μH	±5%	crystal filter matching ind., not needed if FIL 1 is ceramic type
L0	0603	10 nH	±5%	VCO tank inductor
L1	0603	15 nH	±5%	LNA output tank inductor
LRX2	0603	56 nH	±5%	RX impedance matching inductor
LTX0	0603	15 nH	±5%	TX impedance matching inductor
LTX1	0603	27 nH	±5%	TX impedance matching inductor
VD1	SOD-323	BB639		VCO tank varactor diode
XTAL	HC49 SMD	8.0000 MHz ±10ppm calibr. ±20ppm temp.		fundamental-mode crystal, C _{load} = 10 pF to 15pF, C _{0,max} = 7 pF, R _{m,max} = 70 Ω
CERFIL	leaded	SFKLA10M7NL00 @ B _{IF2} = 30 kHz		ceramic filter from Murata, or equivalent part
FIL1	HC-49/U	ECS-10.7-7.5B @ B _{IF2} = 7 kHz		one half (2 poles) of 4-pole crystal filter from ECS, or equivalent part; only required for the Fig. 6 schematic
FIL2				
CERDIS	SMD	CDSCB10M7GA136		ceramic discriminator from Murata, or equivalent part

References

- [1] Ulrich L. Rohde: "Microwave and Wireless Synthesizers", John Wiley & Sons, New York, 1997
- [2] Floyd. M. Gardner: "Phaselock Techniques", John Wiley & Sons, New York, 1979
- [3] Behzad Razavi: "Monolithic Phase-Locked Loops and Clock Recovery Circuits - Theory and Design", IEEE Press, 1996
- [4] J. Craninckx and M. Steyaert: "A Fully Integrated CMOS DCS-1800 Frequency Synthesizer", IEEE J. Solid-State Circuits, vol. 33, pp. 2054-2065, Dec. 1998

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