

TH7122 and TH71221 High Speed Data Communication

1 Introduction to Direct Modulation

The data sheet for the TH7122x transceiver shows FSK generation by switching the load capacitance of the crystal. Since the data signal modulates the reference frequency of the PLL we can call it **Indirect Modulation**. This method works well for data rates up to about 20kbps NRZ (non-return to zero) code or 10kbps RZ (return to zero) code and it has the advantage that the FSK response is down to DC. The drawback is that the PLL bandwidth must be about 5 times the modulation frequency f_m so the reference frequency f_R must be high to suppress the reference spurs sufficiently. As a rule of thumb the reference frequency of the PLL should be at least 10 times the loop bandwidth. Since the reference frequency is equal to the channel spacing in an integer-N PLL as used in the TH7122x, the transmitter can only set a limited number of different channels. For a data rate of 10kbps RZ, the channels should thus be spaced $\geq 500\text{kHz}$.

If high speed data transmission (i.e. high FSK data rates) or small channel spacing is desired, another technique should be used. This method is called **Direct Modulation** of the VCO because the VCO control voltage is combined with the modulation signal in order to modulate outside the loop bandwidth. In this case, the PLL does not track on the modulation signal. Therefore, is necessary to use a small PLL bandwidth and to modulate the VCO outside the loop bandwidth. As a rule of thumb the lowest data signal frequency should be 10 times higher than the loop bandwidth. The only drawback is that the FSK response does not extend to DC (unless it is combined with modulation of the reference). In this case, the data format should not contain a DC component. A bi-phase or Manchester code can be used. If a data burst using NRZ code is used, the ratio of 1's to 0's must be kept small. The channel switching time also increases because of the smaller PLL bandwidth.

2 PLL setup

In order to design the PLL filter, it is first necessary to know the phase detector constant and VCO tuning sensitivity around the desired frequency. There are two ways to determine K_{VCO} :

1. Tune the VCO with a variable voltage from a potentiometer (e.g. 10k Ω) or power supply and measure the output frequency with a counter or spectrum analyzer. This can be done by simply connecting the variable voltage via a 100k Ω resistor to pin 23 of the TH7122x. Using the software for programming the TH7122x with a personal computer, set it to transmit mode, VCOCUR to "11 - high2 current" and PACTRL to '1' so the PA is always on. Adjust the tuning voltage and measure the output frequency.

2. Set-up the TH7122x to operate at the desired frequency in transmit mode using the loop filter on the evaluation board. Connect a high-impedance digital voltmeter to pin 23, the charge pump output. Using the TH7122x software, set the transmitter to frequencies around the operating frequency, and measure the tuning voltage at each frequency. Note capacitive and resistive loading at pin 23 should be as low as possible since this node influences the over-all stability of the PLL directly.

A tuning curve taken on a 433.92MHz evaluation board looks is shown in **Fig. 1**. In this example it can be seen that the slope of the tuning voltage around 434MHz is typically about 22MHz/Volt. Expressed in an angular relation the K_{VCO} yields in

$$K_{VCO} = 2\pi \cdot 22 \frac{\text{MHz}}{\text{V}} = 138.23 \cdot 10^6 \frac{\text{rad}}{\text{s}} \frac{1}{\text{V}}$$

It should be noted that the VCO gain also highly depends on the layout of the PCB. Every additional parasitic capacitive loading of the VCO tank will lower the tuning range of the internal varactor diode and therefore the gain of the VCO.

A second design parameter is the gain of the phase detector K_{PD} . This parameter is proportional to the charge pump current I_{CP} which is $260\mu A$ by default. The charge pump current can be changed by setting the CPCUR bit in the 'A' word register. The phase detector constant is expressed as

$$K_{PD} = \frac{I_{CP}}{2\pi} = 41.38 \frac{\mu A}{rad}$$

As we will see below the 2π term cancels out since K_{PD} and K_{VCO} are always multiplied together.

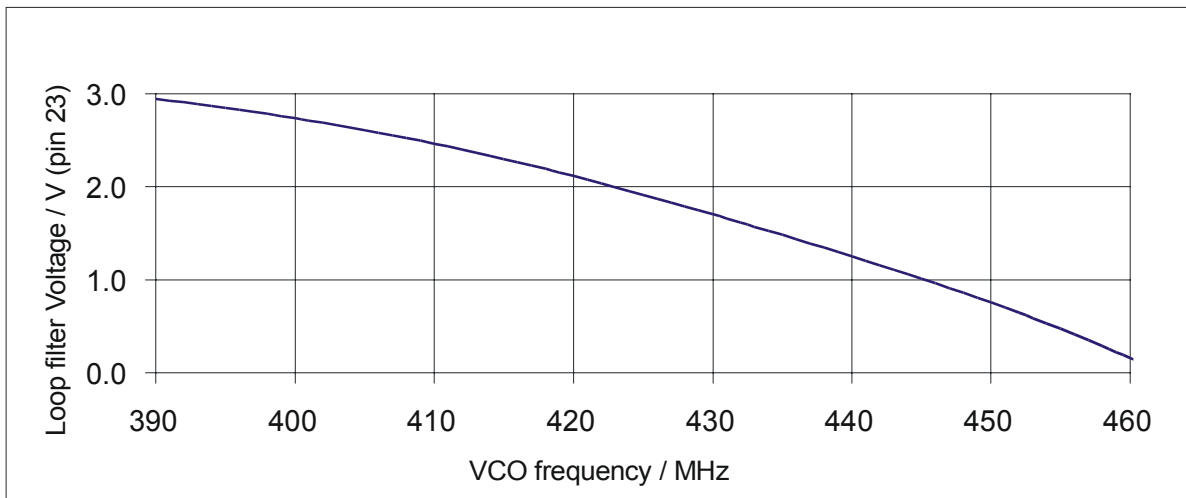


Fig. 1: TH7122 VCO tuning curve for 430MHz center frequency

The recommended loop filter topology is a 2nd order as depicted in **Fig. 2**. From the filter transfer function $F(s)$ we can obtain a zero and a non-DC pole frequency¹:

$$\omega_z = \frac{1}{R_F \cdot C_{F1}} \qquad \omega_p = \frac{C_{F1} + C_{F2}}{C_{F1} \cdot C_{F2} \cdot R_F}$$

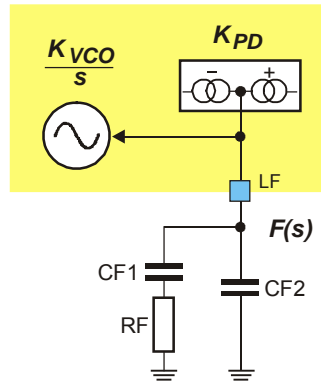
The 3dB bandwidth of the PLL in a closed loop configuration is approximately the transit frequency ω_T of the loop filter. Since C_{F2} is much smaller than C_{F1} in most of the cases, ω_T can be approximated as described in [4]:

$$\omega_T \approx \frac{K_{PD} \cdot K_{VCO} \cdot R_F}{N} \cdot \frac{C_{F1}}{C_{F1} + C_{F2}} \approx \frac{K_{PD} \cdot K_{VCO} \cdot R_F}{N}$$

¹ Investigation of the details of the PLL behaviour would require more space than this application note allows. A more detailed analysis of the PLL behaviour can be found in references [1-3].

Where N represents the value of the feedback divider. For a stable loop the available phase margin is of importance. It should be between 45 and 70 degrees. To ensure enough phase margin at the transit frequency ω_T , the zero frequency should be located M times below and the pole frequency M times above ω_T . As mentioned in [4] a factor M of four gives a phase margin of approximately 60 degrees. With M = 2.5 the phase margin will be approximately 45 degrees.

Fig. 2: 2nd order Loop filter



By using these equations the loop-filter elements can be easily obtained:

$$R_F = \frac{N}{K_{PD} \cdot K_{VCO}} \cdot \omega_T$$

$$C_{F1} = \frac{M}{R_F \cdot \omega_T}$$

$$C_{F2} = \frac{1}{M \cdot R_F \cdot \omega_T}$$

This approximation is quite accurate for calculating the loop filter elements. Normally the step size between the available component values is larger than the error using this calculation method, so that there is no need to use the more complex exact formulas. Nevertheless the exact calculation can be found in [1-3].

Example: If a channel step size of 100kHz is used, a feedback divider of N = 4340 is necessary to achieve a desired operating frequency of 434MHz. Assume a narrow loop frequency, ω_T of about $2\pi \cdot 250$ Hz because of the external VCO modulation. In case of direct modulation of the VCO as a rule of thumb the lowest data signal frequency should be 10 times higher than the loop frequency. To insure loop stability we want a phase margin of about 45 degrees, so the factor M is 2.5. With the equations above and the calculated gains K_{PD} and K_{VCO} the loop filter elements result in:

$$C_{F1} = 1.2 \mu\text{F} \quad C_{F2} = 220 \text{ nF} \quad R_F = 1.2 \text{ k}\Omega$$

As shown in **Fig. 3** the modulation is applied through the parallel combination of C_{M1} and R_{M1} . C_{M1} is required to compensate for the parallel RC time constant $C_{F2} \cdot R_F$. So the following relationship should be fulfilled:

$$R_{M1} \cdot C_{M1} = R_F \cdot C_{F2}$$

Knowing the slope of the VCO control voltage, R_M can be calculated:

$$R_{M1} = R_F \left(\frac{V_{DTAH} \cdot K_{VCO}}{4\pi \Delta f} - 1 \right)$$

Where V_{DTAH} is the high level of the data input signal and Δf the FSK peak deviation.

3 Receiver Set-Up

The standard receiver circuit used in the data sheet works fine up to about 40kbps NRZ, but needs to be modified for higher data rates. Since the OUT_DEM (pin 6) has a 275k Ω output resistance, any stray capacitance on the output will limit the frequency response, so it needs to be loaded to reduce its equivalent resistance. Since the nominal output voltage from the demodulator is $\frac{1}{2}$ VCC, equal resistors to ground and VCC should be used. These are shown as R_{L1} and R_{L2} in **Fig. 3**.

The bandwidth of CERRES, the FM discriminator resonator, is quite small when the load resistor, R_P is 10k. For low data rates, this is satisfactory, but for a modulating frequency of 50kHz and above it results in a loss of signal and low detector output. For modulating frequencies of 115kHz, R_P was made 2.2k Ω to get a higher detector frequency response.

The overall result with the receivers shown in **Fig. 3** is a sensitivity of -95dBm (4 μ V) for a BER of about $450 \cdot 10^{-6}$ at 115kHz modulating frequency.

One note when setting up the receiver: In the standard evaluation boards which are set-up for FSK modulation by crystal pulling via C_{X1} and C_{X2} , the reference oscillator is either above or below the center frequency depending on the state of the FSK_SW on pin 11. In receive mode, the on-chip FSK modulation switch on pin FSK_SW is off, so the crystal oscillator is above the center frequency. If the VCO is below the incoming frequency, the intermediate frequency (IF) is low by the FSK offset frequency. For this reason, the discriminator resonator must be tuned low to operate properly in receive. CP0 across the resonator tunes the discriminator.

When using direct VCO modulation the crystal load capacitor C_{X1} is set such that the crystal oscillator and hence the VCO operates at the center of the channel. Therefore, the IF will also be at its center frequency (10.7MHz). Because of this, C_{P0} must be reduced to tune the discriminator. In this case, it has been changed to 10pF.

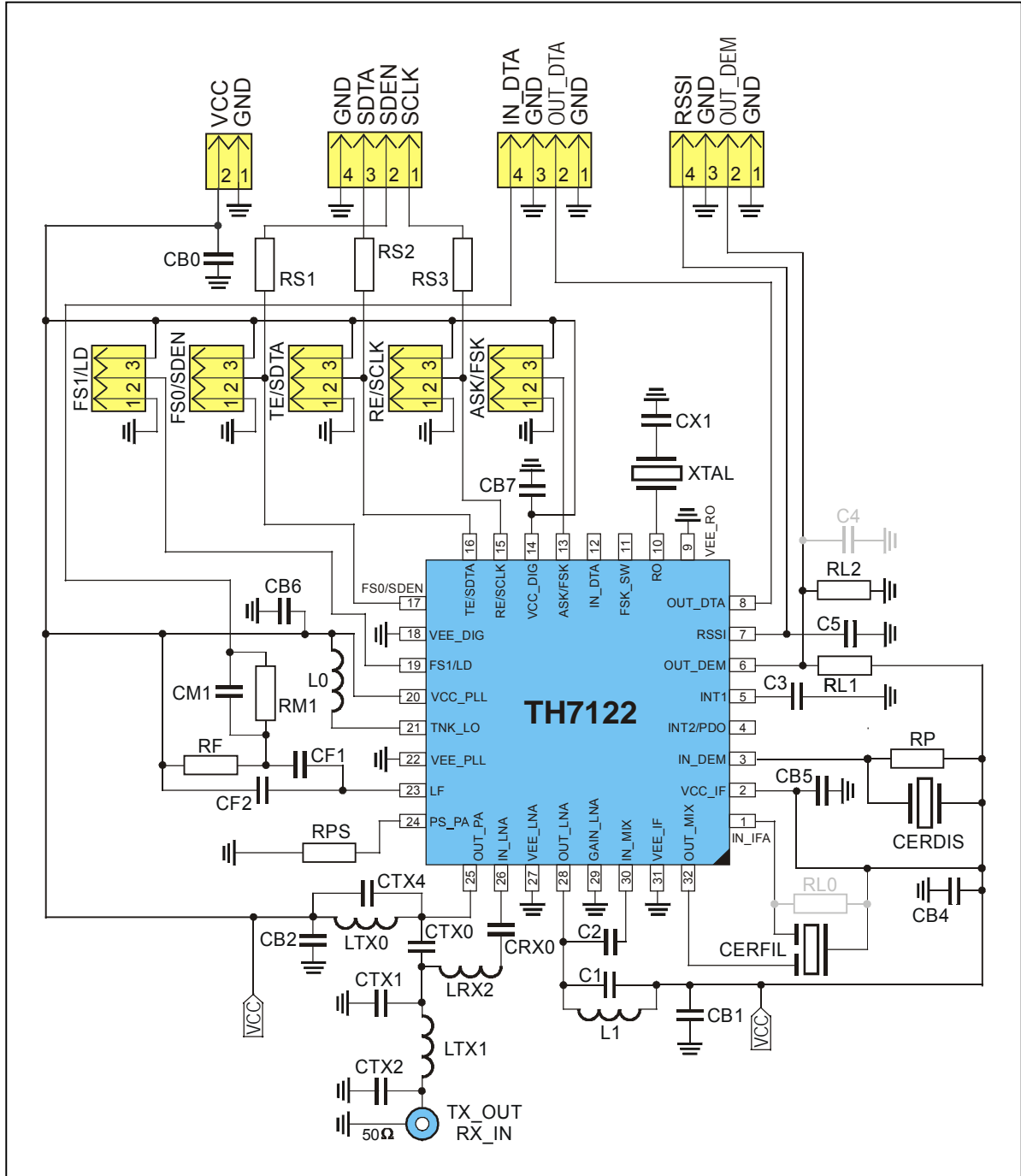


Fig. 3: TH7122x circuit schematic for direct VCO modulation

3.1 Component Values for Fig. 3

Part	Size	Value @ 315 MHz	Value @ 433.92 MHz	Value @ 868.3 MHz	Value @ 915 MHz	Tol.	Description	
C1	0603	5.6 pF	4.7 pF	1.5 pF	1.0 pF	±5%	LNA output tank capacitor	
C2	0603	1.5 pF	1.5 pF	1.5 pF	1.5 pF	±5%	MIX input matching capacitor	
C3	0805	10 nF	10 nF	10 nF	10 nF	±5%	data slicer capacitor	
C4	0805	0 – 39 pF	0 – 39 pF	0 – 39 pF	0 – 39 pF	±10%	demodulator output low-pass capacitor, optionally	
C5	0805	1.5 nF	1.5 nF	1.5 nF	1.5 nF	±10%	RSSI output low pass capacitor	
CB0	1210	10 μF	10 μF	10 μF	10 μF	±20%	de-coupling capacitor	
CB1	0603	330 pF	330 pF	330 pF	330 pF	±10%	de-coupling capacitor	
CB2	0805	330 pF	330 pF	330 pF	330 pF	±10%	de-coupling capacitor	
CB4	0603	10 nF	10 nF	10 nF	10 nF	±10%	de-coupling capacitor	
CB5	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor	
CB6	0603	100 pF	100 pF	100 pF	100 pF	±5%	de-coupling capacitor	
CB7	0603	100 nF	100 nF	100 nF	100 nF	±10%	de-coupling capacitor	
CF1	0805	TBD	1.2 μF	1.2 μF	TBD	±5%	loop filter capacitor	
CF2	0603	TBD	220 nF	220 nF	TBD	±5%	loop filter capacitor	
CM1	0603	TBD	390 pF	390 pF	TBD	±5%	modulation capacitor	
CX1	0805	TBD	33 pF	33 pF	TBD	±5%	RO capacitor for FSK	
CP0	0805	10 - 12 pF	10 - 12 pF	10 - 12 pF	10 - 12 pF	±5%	CERRES tuning capacitor	
CRX0	0603	100 pF	100 pF	100 pF	100 pF	±5%	RX coupling capacitor	
CTX0	0603	100 pF	100 pF	100 pF	100 pF	±5%	TX coupling capacitor	
CTX1	0805	12 pF	5.6 pF	3.9 pF	3.3 pF	±5%	TX impedance matching capacitor	
CTX2	0805	12 pF	4.7 pF	4.7 pF	4.7 pF	±5%	TX impedance matching capacitor	
CTX4	0603	12 pF	4.7 pF	3.3 pF	3.3 pF	±5%	TX impedance matching capacitor	
RF	0603	TBD	1.2 kΩ	1.2 kΩ	TBD	±5%	loop filter resistor	
RL0	0603	390 Ω	390 Ω	390 Ω	390 Ω	±5%	CERFIL loading, optionally	
RL1	0603	100 kΩ	100 kΩ	100 kΩ	100 kΩ	±5%	demodulator output loading	
RL2	0603	100 kΩ	100 kΩ	100 kΩ	100 kΩ	±5%	demodulator output loading	
RM1	0603	TBD	680 kΩ	680 kΩ	TBD	±5%	modulation resistor, adjust for Δf	
RP	0603	2.2 KΩ	2.2 KΩ	2.2 KΩ	2.2 KΩ	±5%	CERRES loading resistor	
RPS	0603	27 kΩ	33 kΩ	47 kΩ	62 kΩ	±5%	power-select resistor	
RS1...RS3	0603	10 kΩ	10 kΩ	10 kΩ	10 kΩ	±5%	protection resistor	
L0	0603	56 nH	33 nH	3.9 nH	3.9 nH	±5%	VCO tank inductor	
L1	0603	27 nH	15 nH	3.9 nH	3.9 nH	±5%	LNA output tank inductor	
LRX2	0603	100 nH	56 nH	10 nH	10 nH	±5%	RX impedance matching inductor	
LTX0	0603	15 nH	15 nH	3.9 nH	3.9 nH	±5%	TX impedance matching inductor	
LTX1	0603	33 nH	27 nH	8.2 nH	8.2 nH	±5%	TX impedance matching inductor	
XTAL	HC49 SMD	7.1505 MHz (or 8.000MHz) ±20ppm calibration, ±20ppm temperature						fundamental-mode crystal, C _{load} = 10 pF to 15pF, C _{0, max} = 7 pF, R _{m, max} = 70 Ω
CERFIL	SMD type	SFECV10M7JA00 @ B _{IF2} = 150 kHz, ±40kHz						ceramic filter from Murata, or equivalent part
CERDIS	SMD type	CDSCB10M7GA136						ceramic discriminator, from Murata, or equivalent part

Your Notes

References

- [1] Ulrich L. Rohde: "Microwave and Wireless Synthesizers", John Wiley & Sons, New York, 1997
- [2] Floyd. M. Gardner: "Phaselock Techniques", John Wiley & Sons, New York, 1979
- [3] Behzad Razavi: "Monolithic Phase-Locked Loops and Clock Recovery Circuits - Theory and Design", IEEE Press, 1996
- [4] J. Craninckx and M. Steyaert: "A Fully Integrated CMOS DCS-1800 Frequency Synthesizer", IEEE J. Solid-State Circuits, vol. 33, pp. 2054-2065, Dec. 1998

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