

Melexis



INSPIRED ENGINEERING

APPLICATION NOTE

Guidelines for Surface Mount Technology (SMT) soldering
(v1.0)

September 2020

Advanced Customer Solutions

Guidelines for Surface Mount Technology (SMT) soldering

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3. SMT process

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3.2 Component placement

3.3 Reflow soldering

3.4 Solder joint inspection & rework

1. Scope

Family of packages at Melexis from soldering perspective

Surface Mount Devices (SMD)

Through Hole Devices (THD)

Gull wing

Straight leads

Bottom Terminated Component (BTC)

Single Inline Package (SIP)

Hermetic

SOIC

TSSOP

SSOP

SOT

QFP

SOIC

SOT

QFN

DFN

UTDFN

BGA

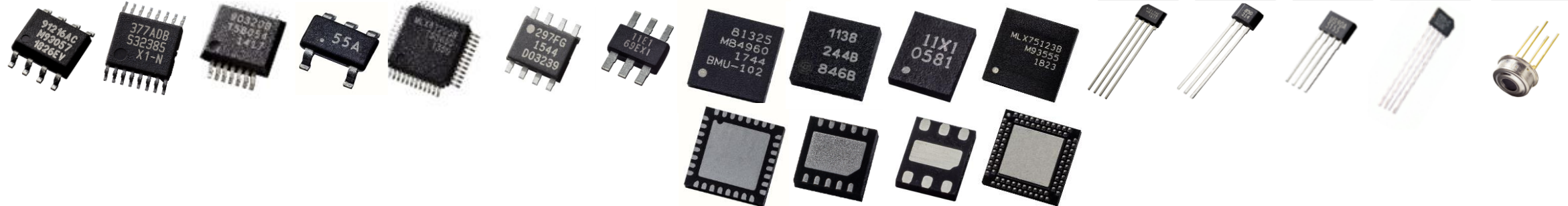
VA

UA

VK

VC

TO-Can



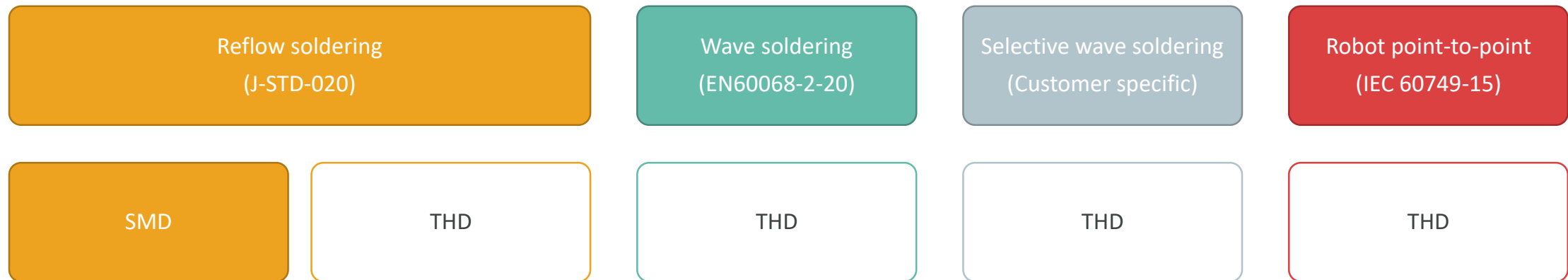
Refer to Annex I for the different abbreviations

Standard packages outlines are defined by the JEDEC committees with a large dimensional window. Melexis PODs (Product Outline Drawing) have narrower tolerances from the qualified manufacturing process of the assembly house, so it is recommended to use these dimensions when designing the PCB.

1. Scope

Applicable soldering methods for Melexis products

Soldering refers to a set of processes for electrically connecting the IC (Integrated Circuit) leads to the PCB (Printed Circuit Board) terminals. Each Melexis product is qualified to one or more methods of soldering following the standards listed below. **For SMD devices, only reflow soldering is applicable, which is covered in this document.** For THD devices, the four soldering methods below are applicable and will be covered in a separate document.



Covered in this AN

The requirements for soldering in J-STD-001 *Requirements for Soldered Electrical and Electronic Assemblies* should be followed independently of the soldering method chosen, as well as IPC-A-610 *Acceptability of Electronic Assemblies* for solder joint quality.

1. Scope

Basic reflow soldering flow for SMT



Reflow soldering can be divided into four main steps:

- 1. Solder paste printing and SPI:** The solder paste contains the solder alloy grains and flux to create the proper metallurgical connection. SPI (Solder Paste Inspection) is a 3D solder paste non-contact measurement of height, area and location, and it is a must to guarantee proper printing parameters and sufficient solder volume in the solder pad.
- 2. Pick and place:** The components are picked from carrier tape and placed onto the solder paste
- 3. Solder reflow:** Both IC (leads and mold package) and PCB are heated so that the solder paste melts and establishes a connection between the pin and the solder pad. Optimal reflow parameters depend on equipment capabilities, PCB and component size and specific characteristics.
- 4. Solder joint inspection:** Automatic Optical Inspection (AOI) checks the solder fillet of the solder joint to verify pin to solder pad connection. Automatic X-ray Inspection (AXI) – applicable for BTC (Bottom Terminated Component) packages - checks the solder joint between the bottom terminal of the IC and the solder pad and measures the percentage of voids.

1. Scope

Moisture sensitivity classification of ICs for SMT reflow soldering

The epoxy mold package of the IC can absorb and retain moisture. During high temperature reflow process, the moisture evaporates and might create pockets of high vapor pressure resulting in structural damage like mold crack or delamination from the leadframe.

To roughly qualify this risk, qualification tests have been defined in J-STD-020 *Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices*. These tests simulate the customer process (also known as pre-conditioning) in a standard way to be able to compare parts and products. The pre-conditioning rules are defined in JESD22-A113H *Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing*.

Melexis devices intended for reflow soldering are qualified in two categories: those sensitive to moisture absorption and the associated risks (MSL3), and those that are not sensitive (MSL1). These tests are applied during product qualification and can be found on the PQR (Product Qualification Report) of the product.

Storage and handling of Melexis devices at customer side should follow guidelines in J-STD-033 *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices* for the respective MSL. Key parameters are printed on the label attached to the product packing. Refer to *Guidelines for storage and handling of plastic encapsulated ICs* on Melexis website for details.

		Pre-conditioning	
Moisture sensitivity	Classification category (MSL)	Moisture loading	Classification reflow peak temperature (Tc)
Non-sensitive to moisture	MSL1	168h 85C/85%	260C/30s (x3 times)
Moisture sensitive	MSL3	96h 85C/60%	260C/30s (x3 times)

As per J-STD-020, preconditioning JESD22-A113H

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3.1 Solder paste printing and inspection

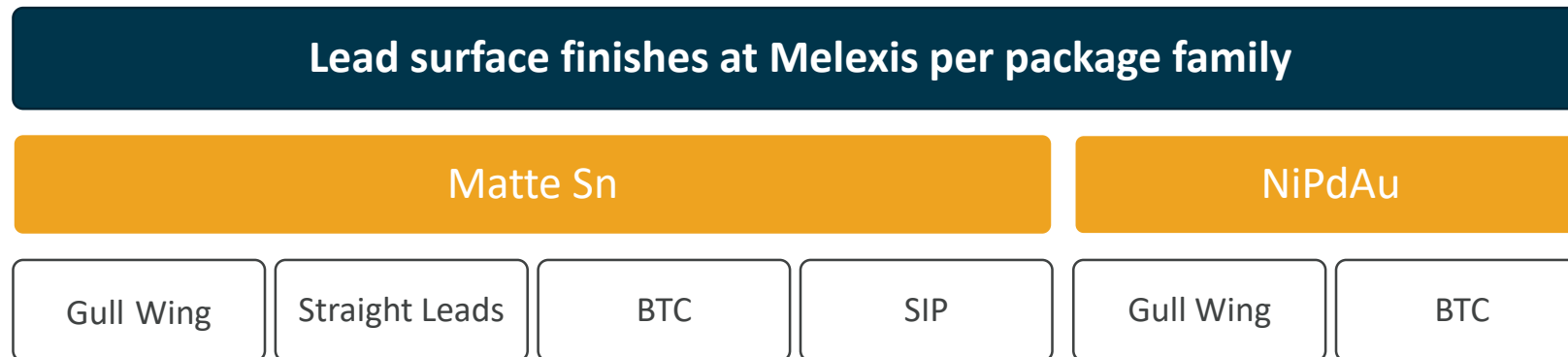
3.2 Component placement

3.3 Reflow soldering

3.4 Solder joint inspection & rework

2.1 Common considerations across package families

Lead surface finish of devices at Melexis



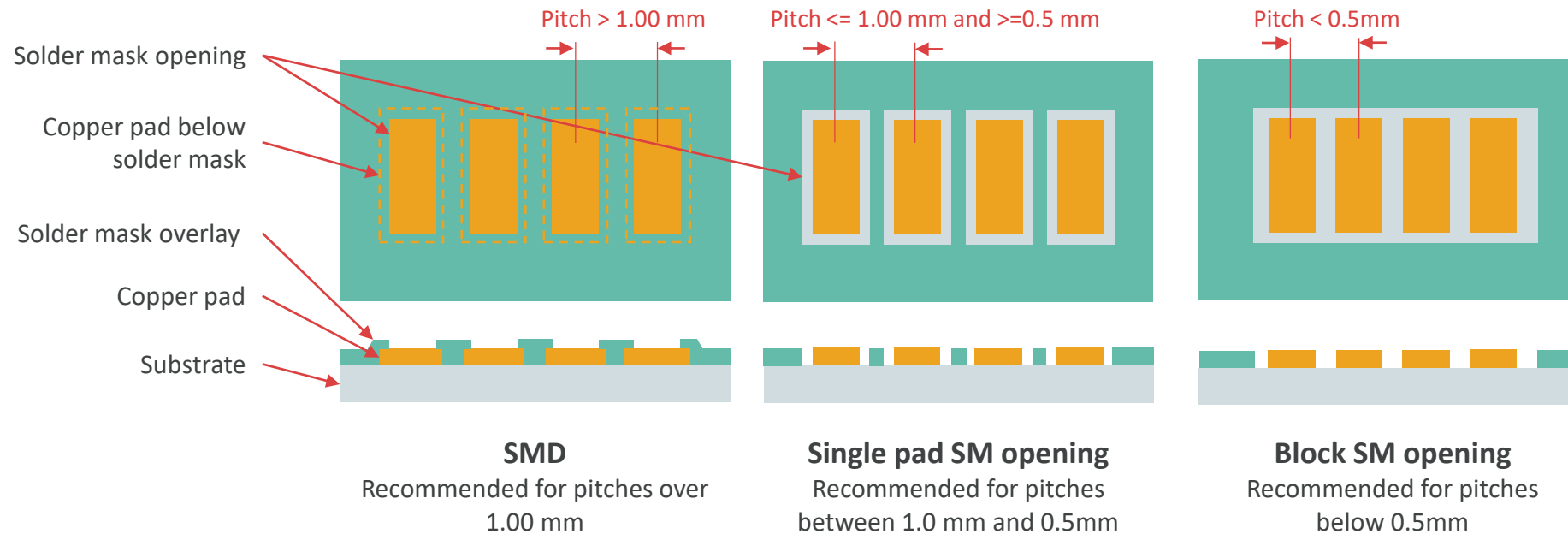
Melexis components are lead-free, but they are backward compatible and well solderable with tin-lead (SnPb) alloys. There are two main lead finishes at Melexis: matte tin (Sn) and Nickel-Palladium-Gold (NiPdAu) finish.

The solderability criteria has been defined in the industry with a guard band:

- ✔ 95% of solderable area wetting by solder (following dip and look test as per J-STD-002 *Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires*), to be met by component supplier.
- ✔ 75% of solderable area of lead to PCB solder joints (following IPC-A-610 *Acceptability of Electronic Assemblies*), to be met by component user soldering on PCB.

2.1 Common considerations across package families

PCB solder pad design



These recommendations are considering a standard solder mask (SM) development accuracy of +/-75um at the PCB house and might be increased or reduced according to the capabilities of the PCB house chosen.

2.1 Common considerations across package families

PCB surface finishes

The surface finish of the PCB protects the copper of the trace while helping improve the wettability of the molten solder to the solder pad. The two main characteristics of the surface finish to take into account from the IC point of view are:

- The planarity of the surface finish, which might impact the quality of the solder joint of packages with low stand-off
- The shelf life of the surface finish, which is usually shorter than the shelf life of the IC.

PCB surface finishes applicable to Melexis packages		
Type	Planarity	Typical shelf Life
OSP	Good	6 months
ENIG	Good	12 months
ENEPIG	Good	12 months
Imm Sn	Good	6 months
Flash Au	Good	12+ months

Note 1: The shelf life reflected here are typical values for the industry, but highly dependent on manufacturer and storage conditions. Contact PCB manufacturer for storage conditions and recommended shelf life for the selected surface finish.

Note 2: HASL and LF HASL are not recommended because of the poor planarity

Note 3: Flash Au (Gold) is an expensive finish

2.1 Common considerations across package families

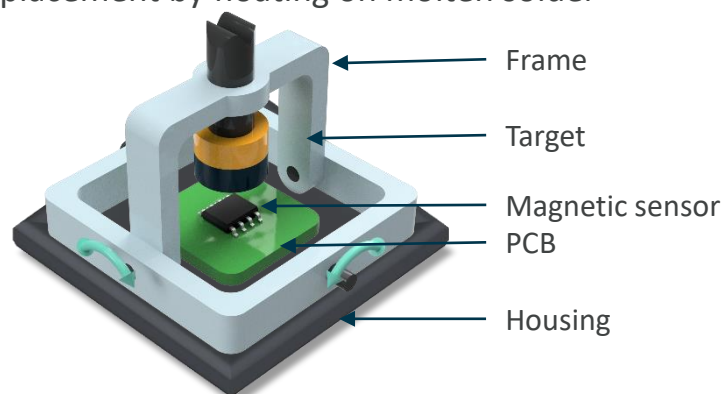
PCB land patterns for high accuracy positioning

PCB land patterns can be calculated following the guidelines in IPC-7351 *Generic Requirements for Surface Mount Design and Land Pattern Standard*. Alternatively, they can usually be found in the datasheet of the product.

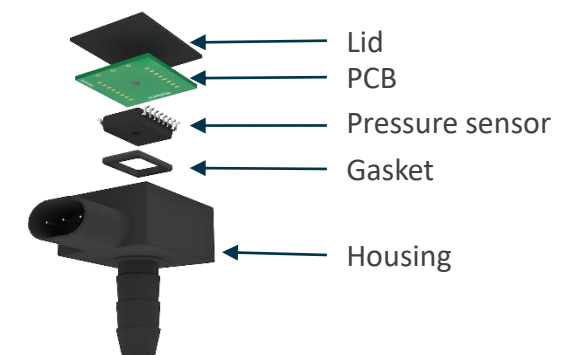
These land patterns take into consideration several tolerances and tend to give wide solder pads: as a consequence, during reflow soldering the package might float on top of the molten solder and shift its designed position. This might have an impact in two sets of products at Melexis:

- **Magnetic sensors:** A misalignment of the package and the target might add an error.
- **Pressure sensors:** A misalignment of the package and the gasket might lead to plugging the pressure port when the gasket opening cannot be enlarged to compensate.

For these two applications, high accuracy positioning is important: the following sections will recommend the minimum solder pad dimensions to reduce the misplacement by floating on molten solder



Alignment of a magnetic sensor and the target (which is fixed with reference to the PCB)



Alignment of a pressure sensor to the gasket (which is fixed with reference to the PCB)

2.1 Common considerations across package families

Stencil design

Stencil design is detailed in IPC-7525 *Stencil Design Guidelines*, and needs to take into consideration all the devices to be mounted on the PCB, as well as several others parameters (speed, pressure and angle of the squeegee, distance to the PCB, transfer coefficient...).

From Melexis ICs point of view, the following two parameters help achieving a reliable strong solder joint:

Recommendation for stencil design from Melexis point of view

Solder paste and stencil thickness

Gull Wing

5 to 6 mil

Straight Leads

5 to 6 mil

BTC

4 to 5 mil

SIP in SMD shape

5 to 6 mil

Ratio of stencil opening to solder pad

Gull Wing

90%

Straight Leads

90%

BTC

90% for 5 mil
100% for 4 mil

SIP

90%

Note: Ratio of stencil opening to solder pad applies to both SMD and NSMD

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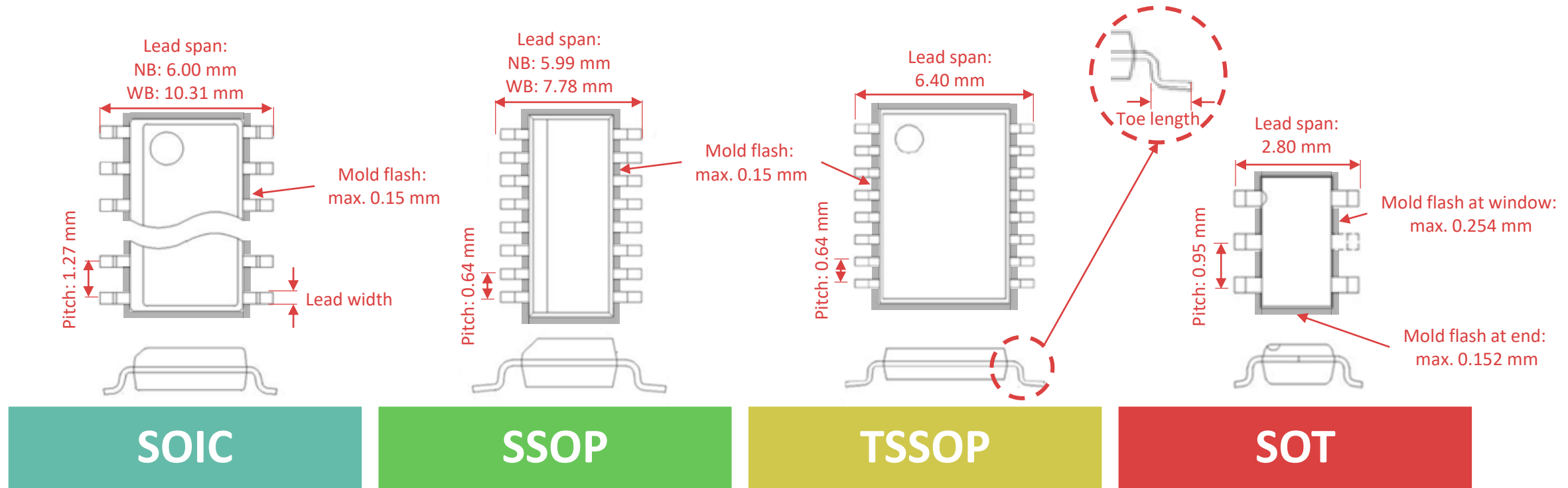
3.3 Reflow soldering

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2.2 Gull wing package family

Gull wing package family

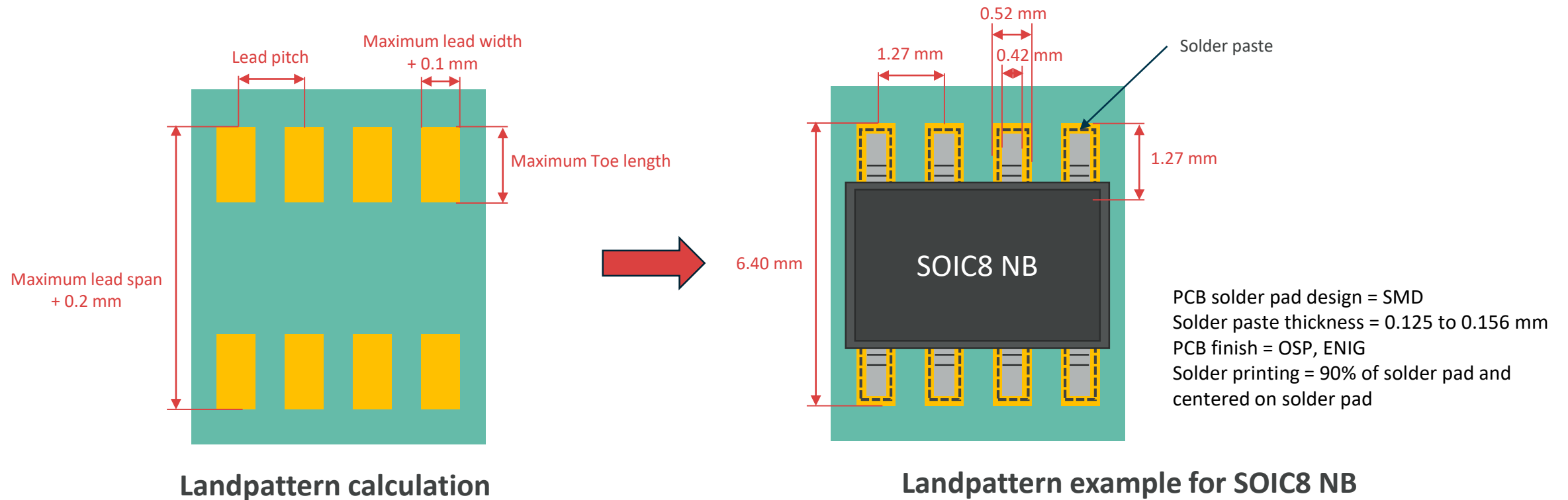
Gull wing packages are so named because, seen from the side and up-down, the pins are similar to the wings of a gull in mid fly. These are JEDEC standard packages, and come in different mold sizes and pin counts.



Refer to the appropriate datasheet for the product's POD

2.2 Gull wing package family

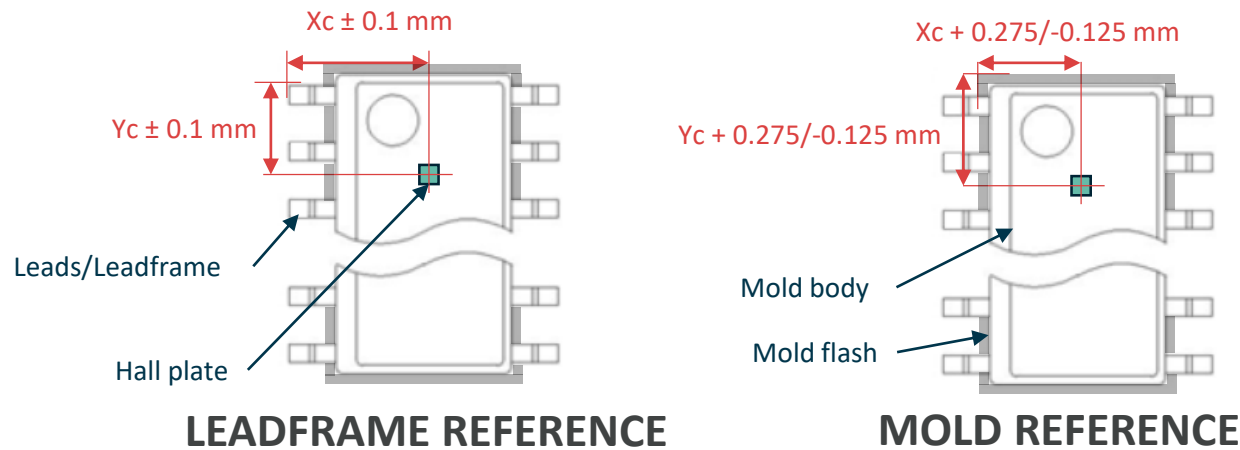
Land patterns for gull wing packages



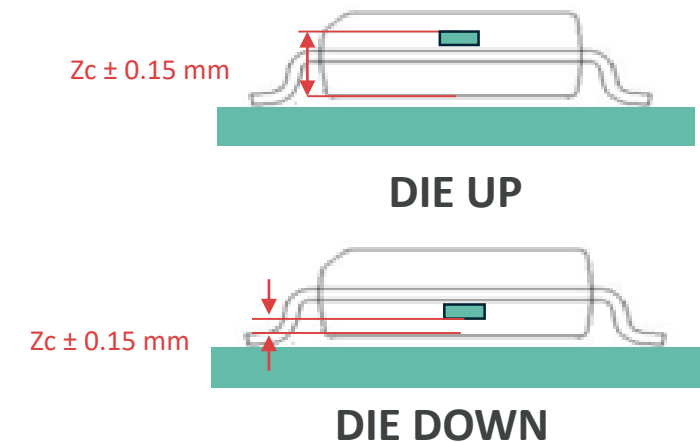
For TSSOP and SSOP with lead pitch 0.64 mm, it is recommended to use NSMD type solder pads with block solder mask opening (depending on the solder mask development capabilities)

2.2 Gull wing package family

Hall plate position tolerance inside gull wing package



*Note: Package floating on solder pads during reflow adds $\pm 50 \mu\text{m}$
(This tolerance is according average placement accuracy of PCB assy process)*



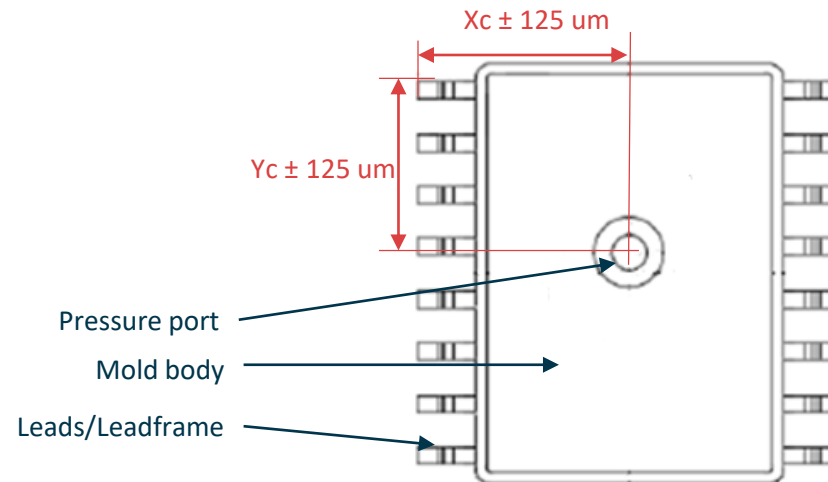
Note: Solder thickness variation will add extra tolerance which depends on solder paste thickness, stencil...

For Hall sensor applications, die magnetic center (Hall plate) shall be centered to the magnetic target. During IC plastic assembly, **the die is placed and optically centered on the leadframe** (die center to leadframe center). The pin outline of the package is a part of the leadframe and therefore is the best reference for PCB design. Alignment of the magnetic center using the mold body adds extra tolerance from the mold body and mold flash and hence is not recommended.

These are best achievable tolerances, which are only needed for high positioning accuracy of certain devices, like magnetic sensor. Refer to the datasheet for the actual X_c , Y_c and Z_c dimensions.

2.2 Gull wing package family

Pressure port position tolerance in gull wing package



Note 1: Package floating on solder pads during reflow adds $\pm 50 \text{ um}$

Note 2: Tolerance for placement of PCB to housing is not taken into account

For pressure sensors the centering is done on the pressure port on mold body for sealing using a gasket. The pressure port is in the mold body and hence it is the best reference.

These are best achievable tolerances, which are only needed for high positioning accuracy of certain pressure sensors. Refer to the datasheet for the actual X_c , Y_c and Z_c dimensions.

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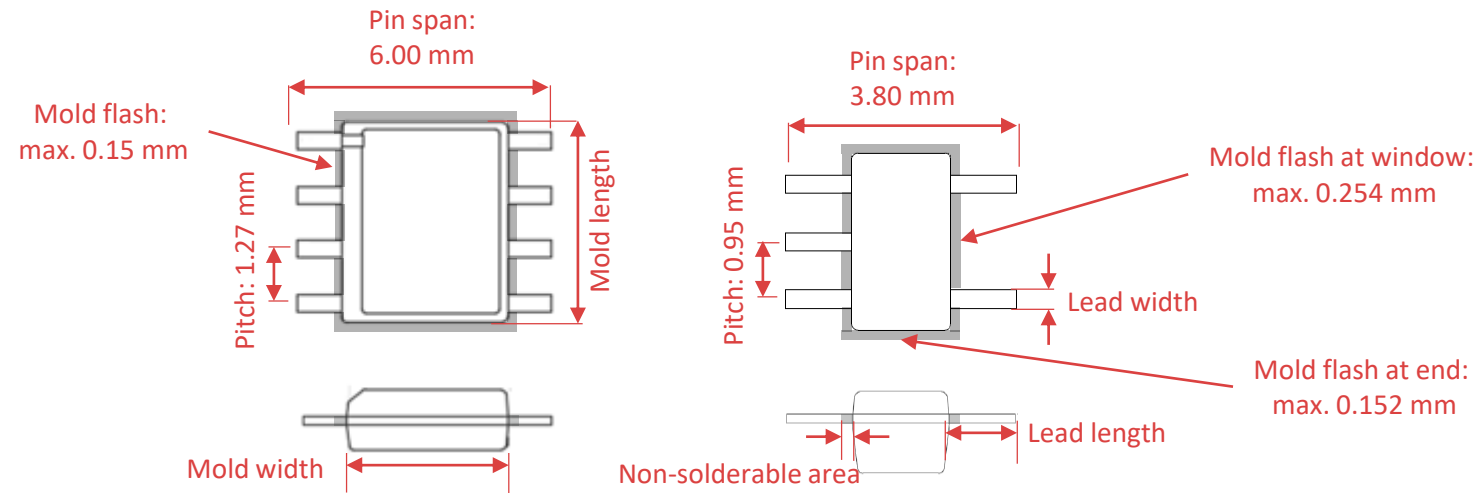
3.3 Reflow soldering

3.4 Solder joint inspection & rework

2.3 Straight leads package family

Straight leads package family

Straight leads packages are gull wing packages that have not gone through lead-forming: the back-end process that gives the pins their gull wing shape. These packages are intended to be placed in the cavity of a PCB to achieve a low profile assembly.



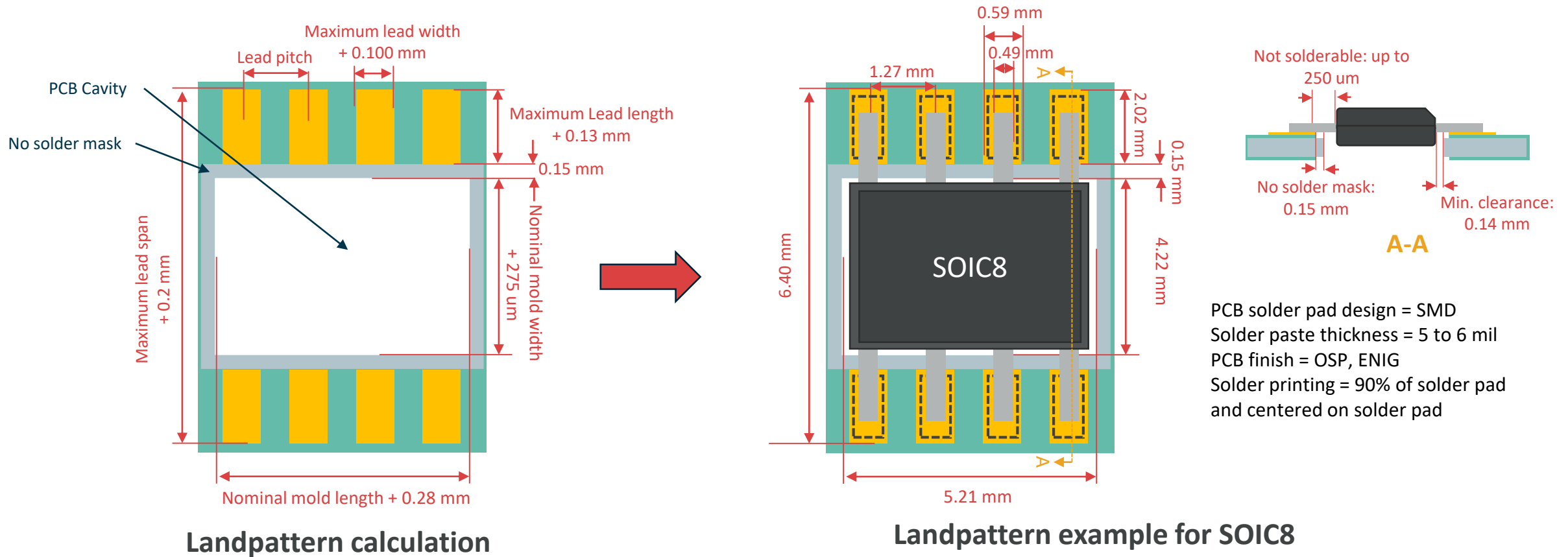
SOIC

SOT

Refer to the appropriate datasheet for the product's POD

2.3 Straight leads package family

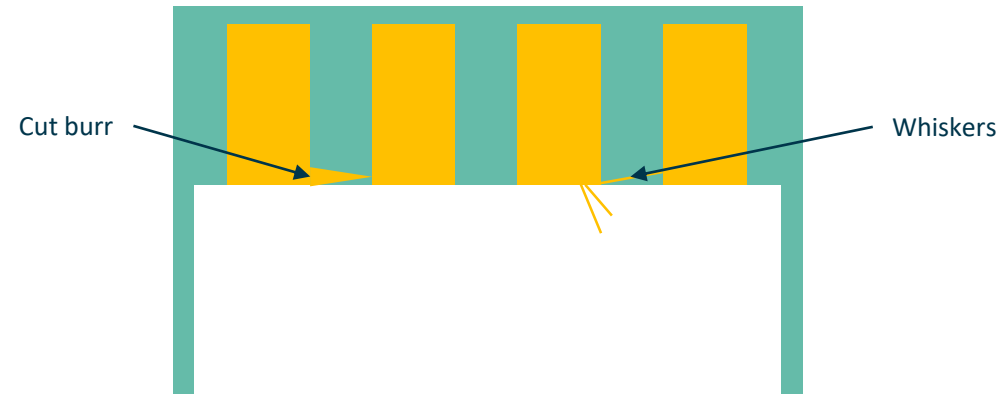
Land patterns for straight leads packages



It is recommended to secure some clearance between the solder pad and the PCB cavity edge to avoid cut burrs and whiskers leading to short-circuits.

2.3 Straight leads package family

Known issues when soldering straight leads packages

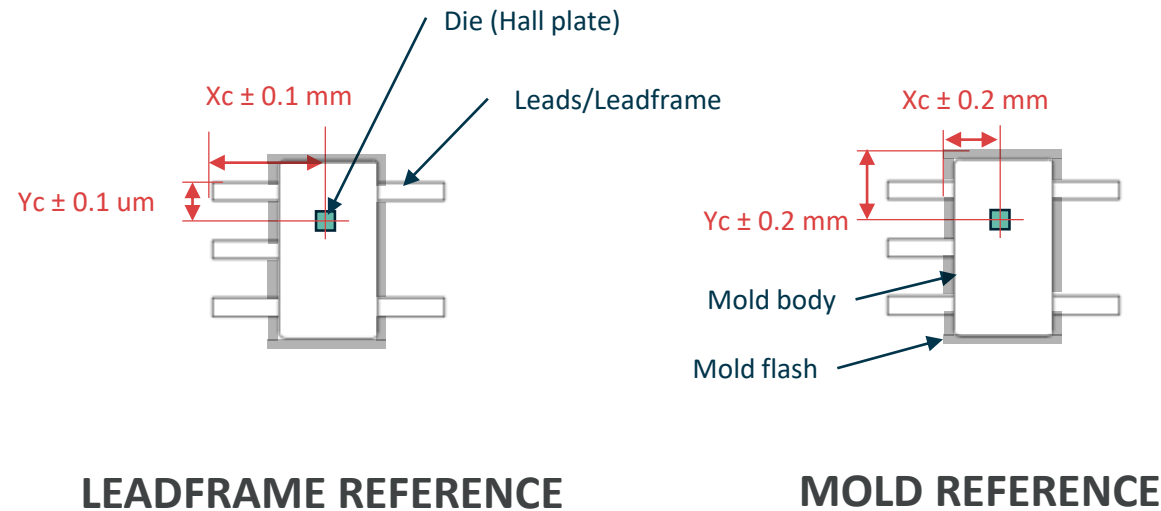


Risk of short by cut burrs or whiskers

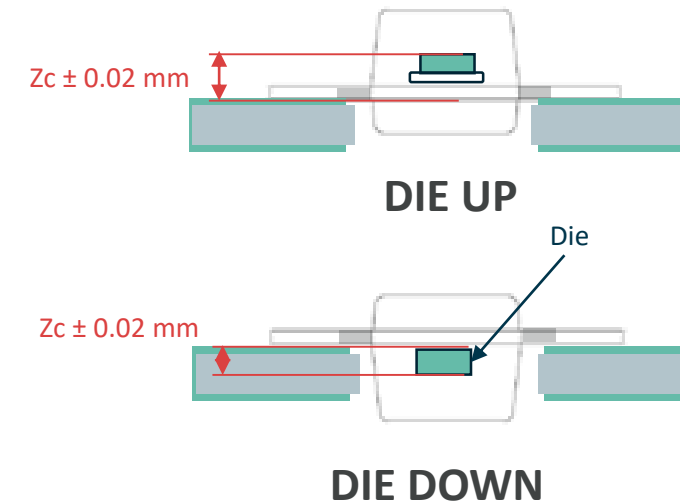
If no clearance is foreseen between the edge of the cavity and the solder pad, cut burrs or whiskers might appear after milling, which might lead to short circuits between pads

2.3 Straight leads package family

Hall plate position tolerance inside straight leads package



*Note: Package floating on solder pads during reflow adds $\pm 50 \text{ um}$
(This tolerance is according average placement accuracy of PCB assy process)*



Note: Solder thickness variation will add extra tolerance which depends on solder paste thickness, stencil...

The die is placed before plastic molding and it is aligned to the pins of the package. Therefore, it is better to use the pins for alignment

These are best achievable tolerances, which are only needed for high positioning accuracy of certain devices, like magnetic sensor. Refer to the datasheet for the actual X_c , Y_c and Z_c dimensions.

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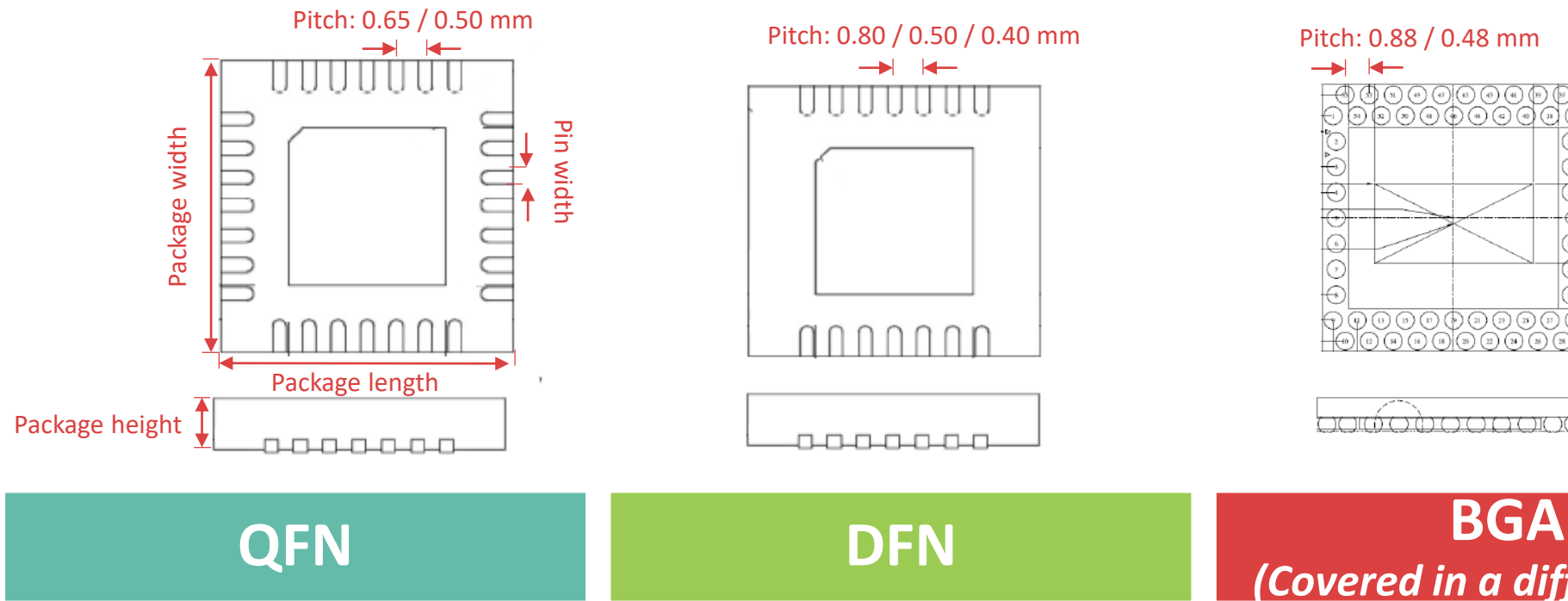
3.3 Reflow soldering

3.4 Solder joint inspection & rework

2.4 BTC package family

BTC package family

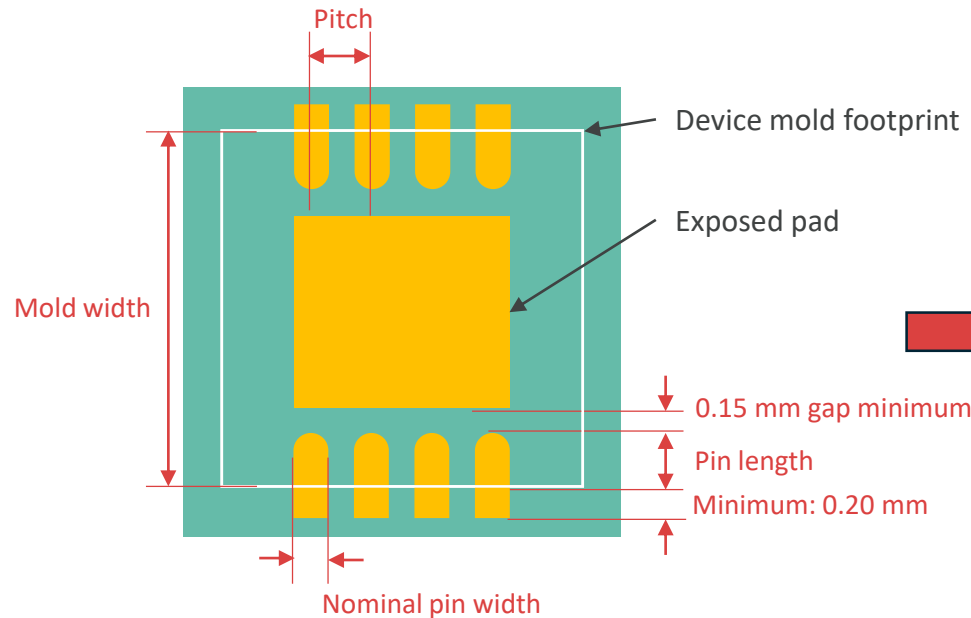
The QFN and DFN packages are of the sawn type: molding is done in a shared cavity for all devices, and then a sawing blade is aligned to the leadframe prior singulation. The accuracy of sawing is ± 50 μm .



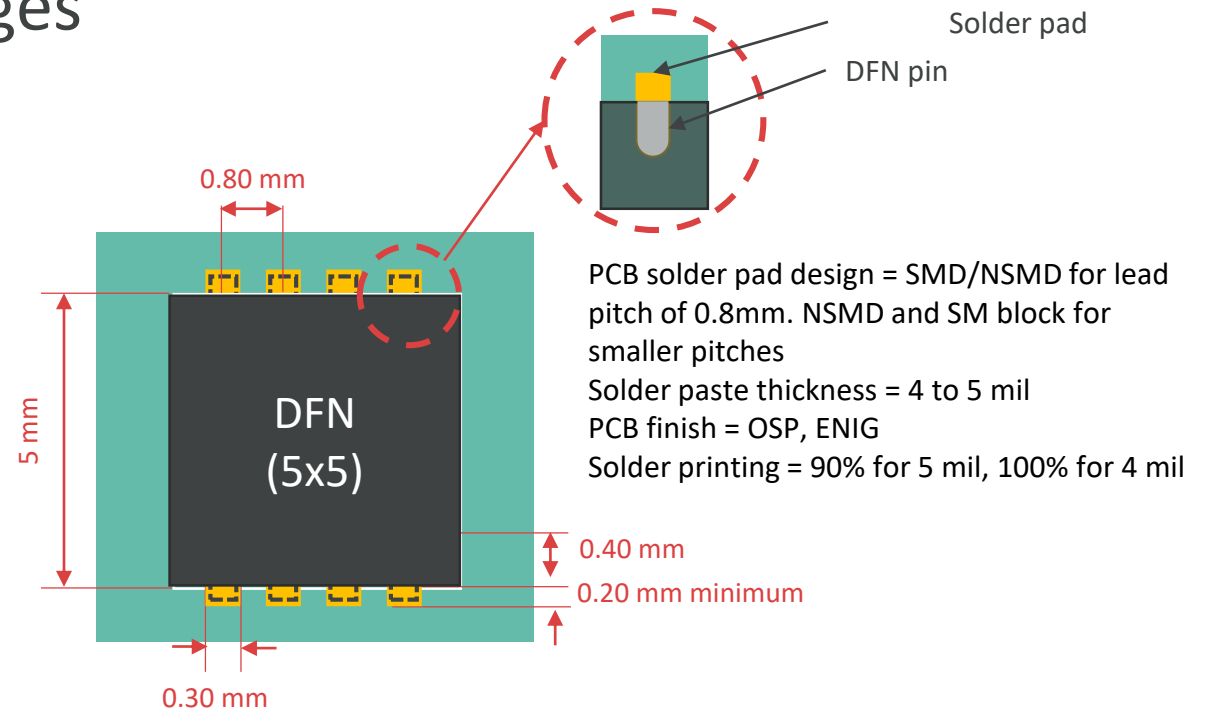
Refer to the appropriate datasheet for the product's POD

2.4 BTC package family

Land patterns for QFN/DFN packages



Landpattern calculation



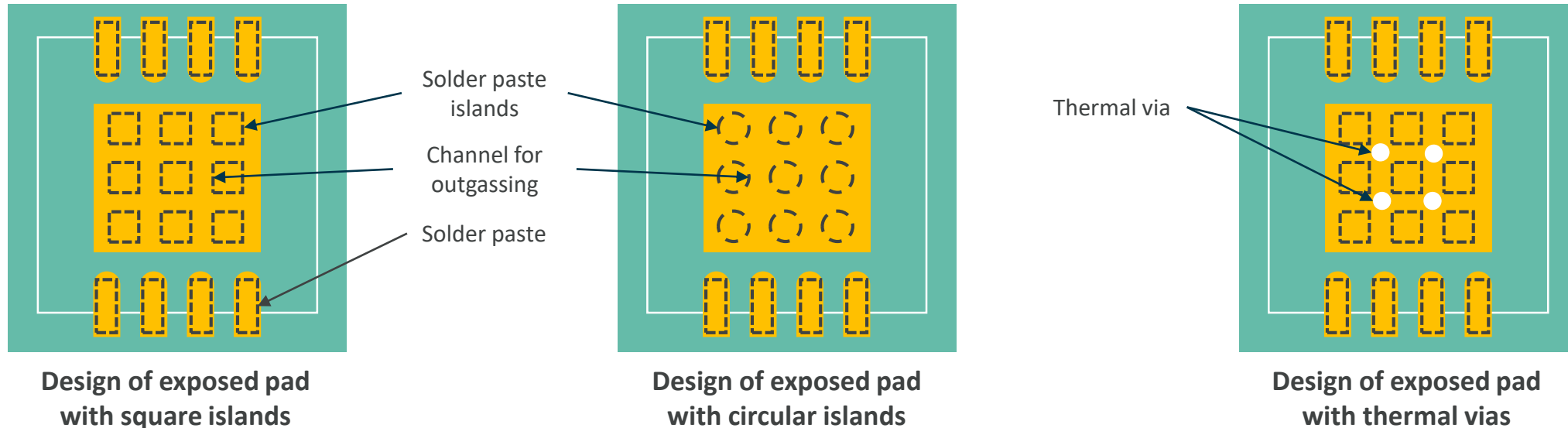
Landpattern example for DFN 5x5

PCB solder pad design = SMD/NSMD for lead pitch of 0.8mm. NSMD and SM block for smaller pitches
 Solder paste thickness = 4 to 5 mil
 PCB finish = OSP, ENIG
 Solder printing = 90% for 5 mil, 100% for 4 mil

If the device has an exposed pad, it is recommended to solder it to the PCB to improve thermal dissipation. Electrical clearances between high voltage pins shall be respected as per IPC 2221 *Generic Standard on Printed Board Design*

2.4 BTC package family

Exposed pad and thermal vias design for QFN/DFN packages



The solder paste (stencil opening) for exposed pad should have channels to help with the outgassing of fluxes during reflow and hence reduce the existence of voids. There are two requirements when designing the islands (square, circular or other shape) for the exposed pad:

- The solder paste of an island should be similar in volume to the solder paste on a single solder pad, and the total area covered of the solder paste for exposed pad should be 40% to 60% of the exposed pad area
- The solder paste in the island should be symmetrical shape so outgassing is the same in X and Y directions

If the application requires thermal vias, it is recommended to place them between the islands to reduce solder loss through the vias, which might lead to voiding in the solder pad. Alternatively, the vias might be plugged with epoxy to avoid solder loss.

2.4 BTC package family

Known issues when soldering QFN/DFN packages

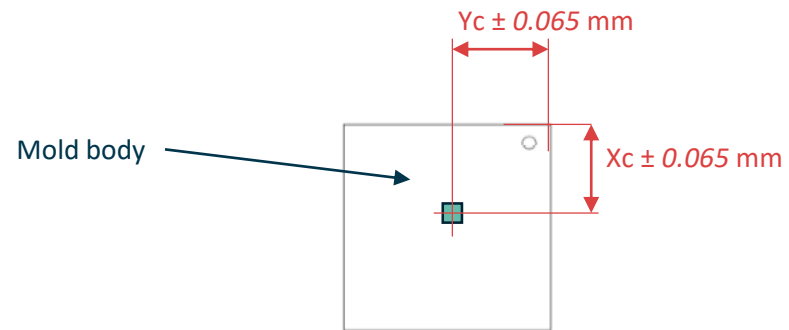


Risk of IC lift or tilt

If the islands in the exposed pad are too big, too much solder paste will be dispensed. After reflow, the IC will be lifted above the solder on the solder pads, or tilted if one side is soldered (but not the other)

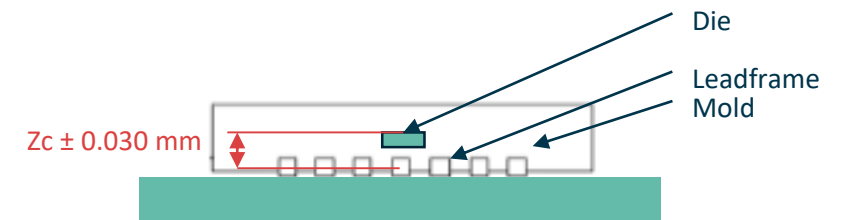
2.4 BTC package family

Hall plate position tolerance inside QFN/DFN packages



MOLD REFERENCE

*Note: Package floating on solder pads during reflow adds $\pm 50 \mu\text{m}$
(This tolerance is according average placement accuracy of PCB assy process)*



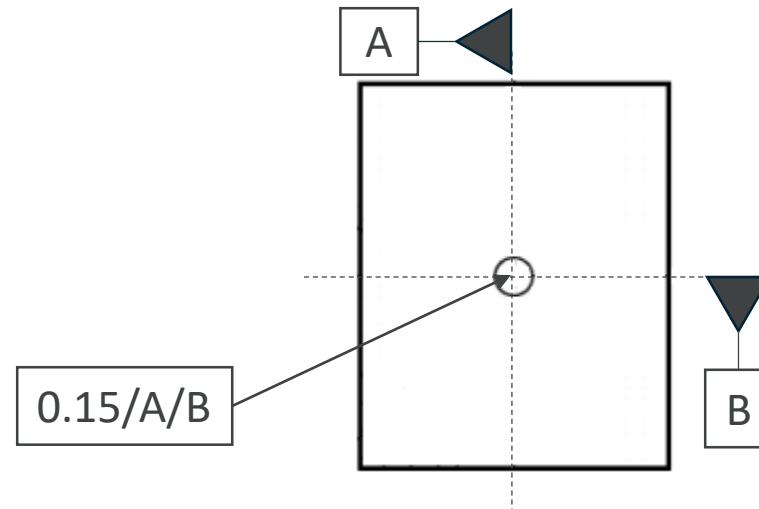
DIE UP

Note: Standoff after soldering adds $\pm 10 \mu\text{m}$

These are best achievable tolerances, which are only needed for high positioning accuracy of certain devices like magnetic sensor. Refer to the datasheet for the actual X_c , Y_c and Z_c dimensions.

2.4 BTC package family

Pressure port position tolerance in QFN package



*Note: Package floating on solder pads during reflow adds $\pm 50 \mu\text{m}$
(This tolerance is according average placement accuracy of PCB Assy process)*

These are best achievable tolerances, which are only needed for high positioning accuracy of certain pressure sensors. Refer to the datasheet for the actual Xc, Yc and Zc dimensions.

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3.2 Component placement

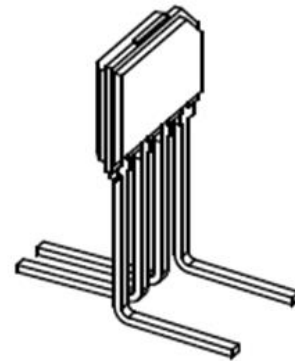
3.3 Reflow soldering

3.4 Solder joint inspection & rework

2.5 SIP package family (in SMD shape)

SIP package family (in SMD shape)

SIP packages are originally intended for through-hole assembly. If the pins are bended 90 degrees, the part can be assembled using surface mount technology. If it is foreseen to do lead forming at customer side, refer to the application note *Guidelines for lead forming of Hall sensors in SIP package*

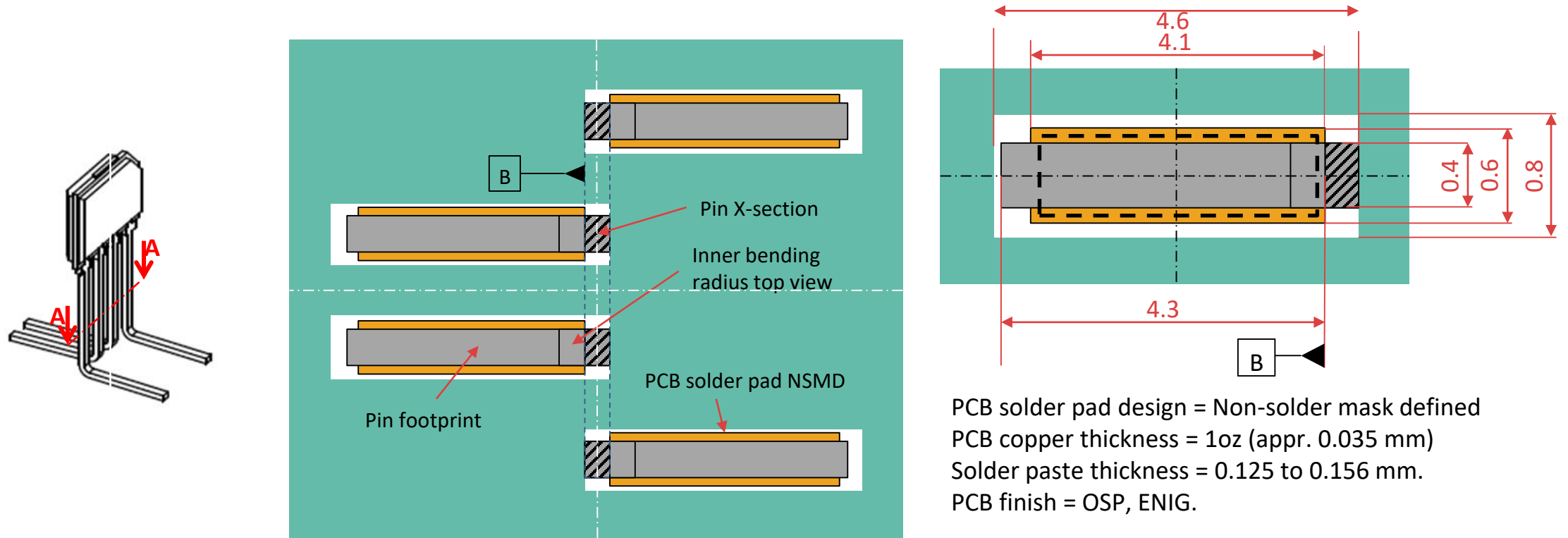


VA in SMD shape

Refer to the appropriate datasheet for the product's POD

2.5 SIP package family (in SMD shape)

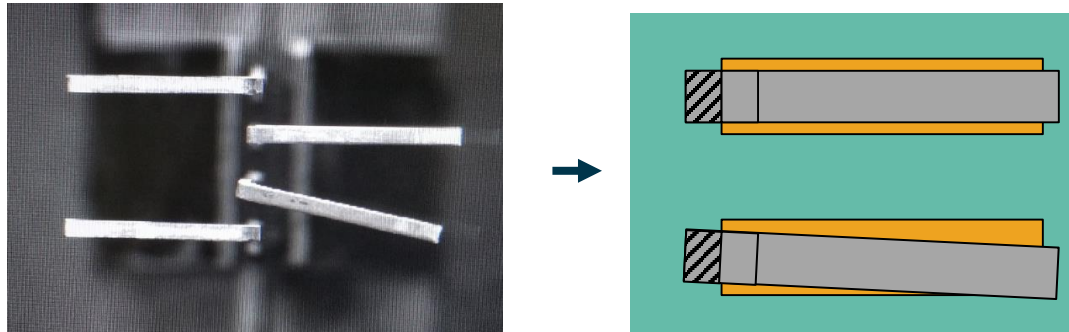
Land pattern design for SIP (VA) packages in SMD shape



Pins might not be completely parallel, so NSMD is recommended to avoid lifting of the pin if it protrudes a little bit from the solder pad. The pin should be longer than solder pad to avoid conflict with the cutting burr

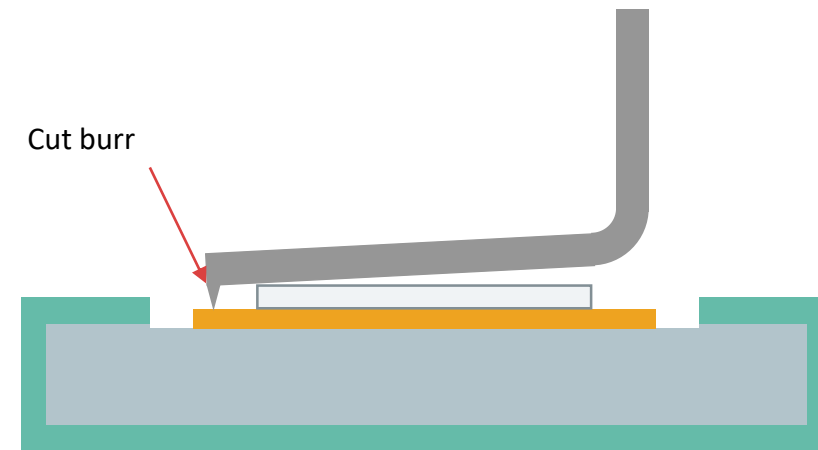
2.5 SIP package family (in SMD shape)

Known issues when soldering SIP in SMD shape



Risk of lead stepping on solder mask (if bending is out of spec)

If SMD solder pads are used, there is a risk that the lead steps on top of the solder mask due to non-parallelity of the leads. This will affect the positioning of the part and potentially the wetting by the solder



Risk of conflict with cut burr

If the solder pad is longer than the pin length, there might be a conflict with the cut burr present in two of the pins. This will affect the positioning of the part and potentially the wetting by the solder

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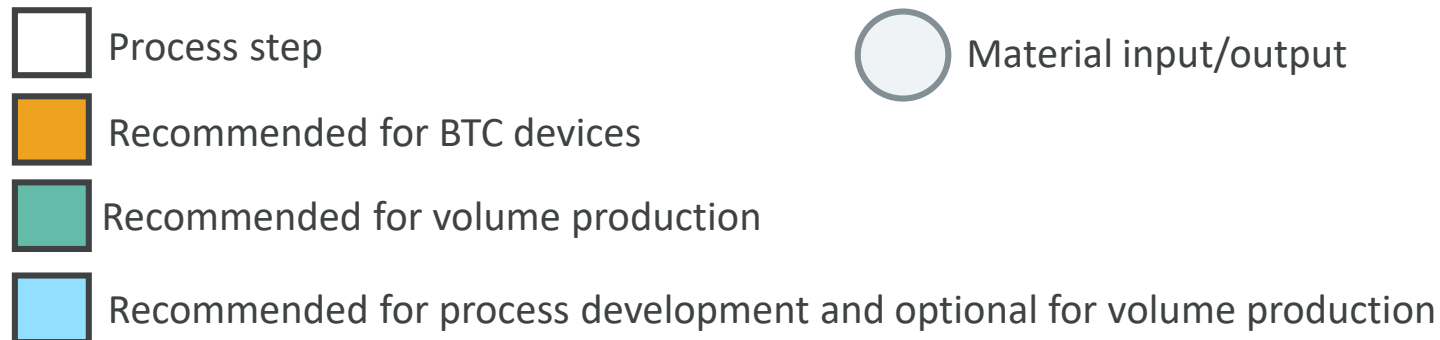
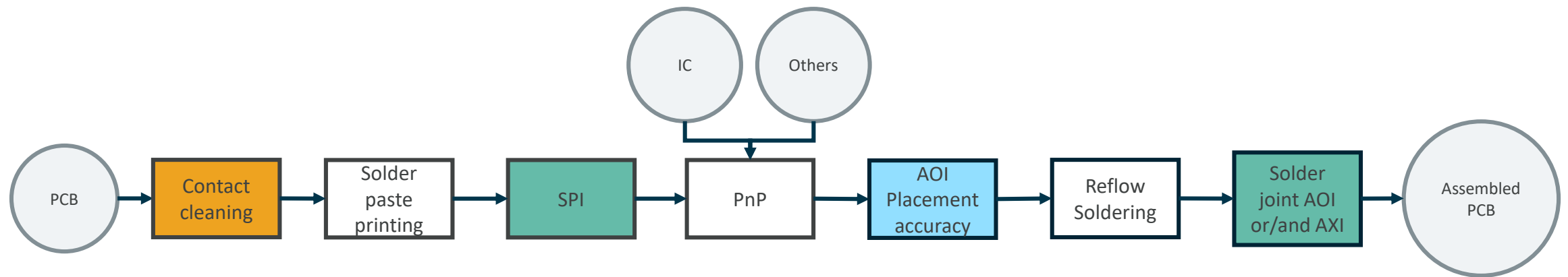
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Reference process flow of a PCB assembly for SMT components



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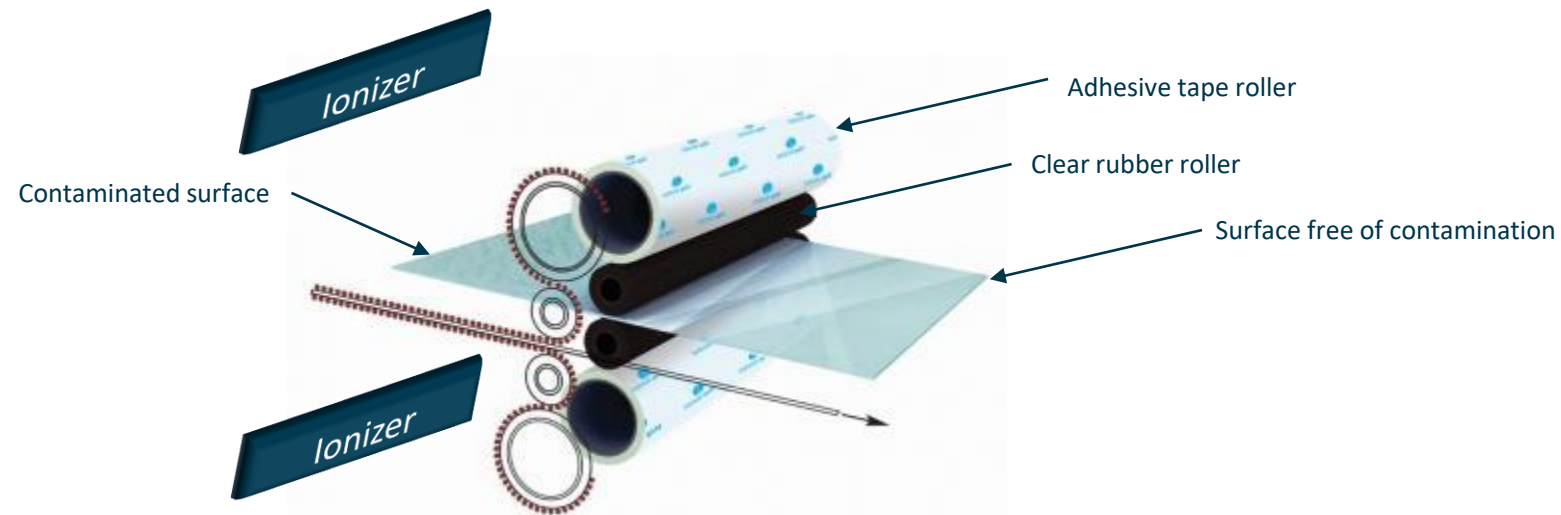
3.2 Component placement

3.3 Reflow soldering

3.4 Solder joint inspection & rework

3.1 Solder paste printing and inspection

Contact cleaning of PCBs for QFN/DFN



Example of PCB contact cleaning

Picture courtesy of [Teknek](#)

QFN/DFN devices have a low-standoff, therefore it is recommended to use a in-line PCB cleaning system to remove any contamination (as well as static charge) and reduce defects. This PCB cleaning system usually consists on two parts:

- Ionized air control which reduces the adhesion of particles by blowing air on the PCB
- Contact cleaning which removes the debris by a roll with tacky rollers on both sides.

3.1 Solder paste printing and inspection

Solder paste composition

Recommendation for solder paste

Flux selection criteria

Solder alloy selection criteria

No clean, Halogen free

Recommended for all packages. For QFN/DFN and open cavity package is a must due to the low standoff where effective cleaning is not possible

No clean, Halide free

It can be used for gull wing, straight leads and SIP in SMD shape packages.

The PCB needs protection from environment to avoid decomposition of the halide compounds left on the PCB, which might lead to corrosion

Water soluble

Not allowed for QFN/DFN

For leaded packages is a must to perform flux wash after reflow

Reflow profile

Shall not exceed classification temperature values of **all the components** as per J-STD-020

Should be compatible with the reflow oven capabilities.

It has to follow the solder paste supplier recommendations

Solder content

Refer to standard J-STD-005

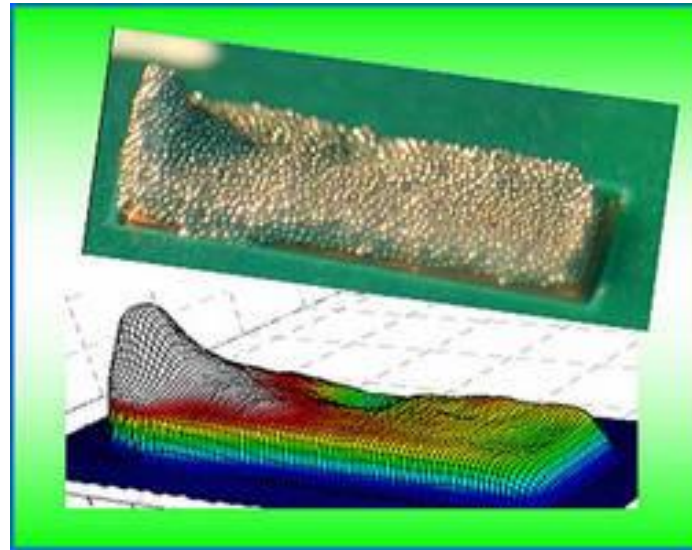
SAC305 could be recommended for all Melexis products

Solder grain size: type 4-5 for QFN/DFN family package, Type 3 and 4 for gull wing, straight leads packages is recommended

Note: Fluxes can be categorized by J-STD-004 Requirements for Soldering Fluxes, and its selection depends on the PCB and component characteristics

3.1 Solder paste printing and inspection

Solder printing and Solder Paste Inspection



Example of solder print inspection

Picture courtesy of [ITW EAE - MPM](#)

Stencil and printing performance can be verified only by SPI (solder paste inspection or surface profile inspection). SPI is strongly recommended to measure X, Y and Z profile of the solder paste and to secure that the required volume has been deposited properly on the whole surface of the PCB panel.

Guidelines for Surface Mount Technology (SMT) soldering

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2.3 Straight leads package family

2.4 BTC package family

2.5 SIP package family (in SMD shape)

3. SMT process

3.1 Solder paste printing and inspection

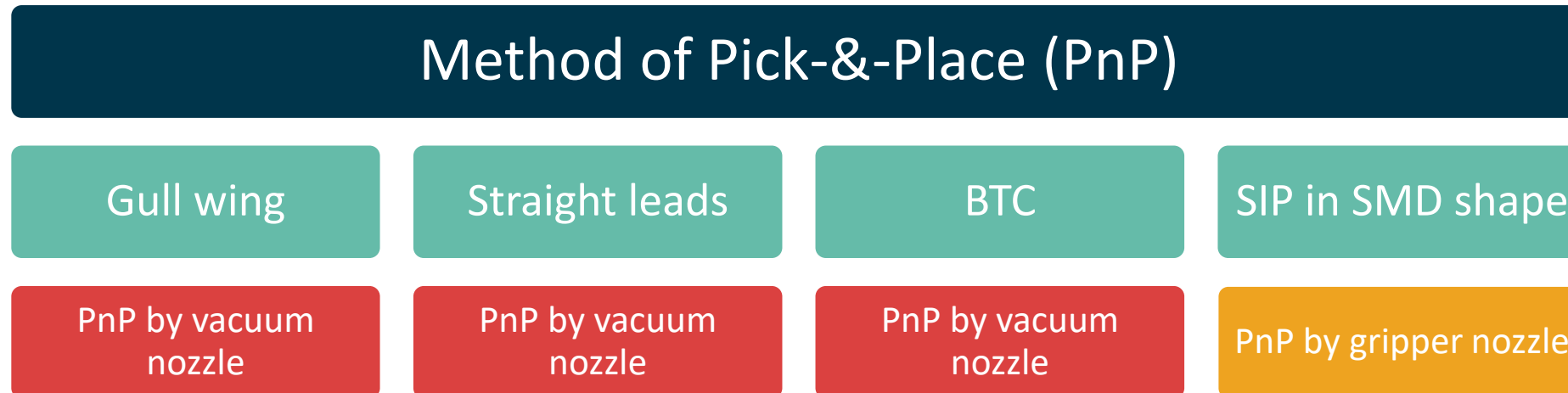
3.2 Component placement

3.3 Reflow soldering

3.4 Solder joint inspection & rework

3.2 Component placement

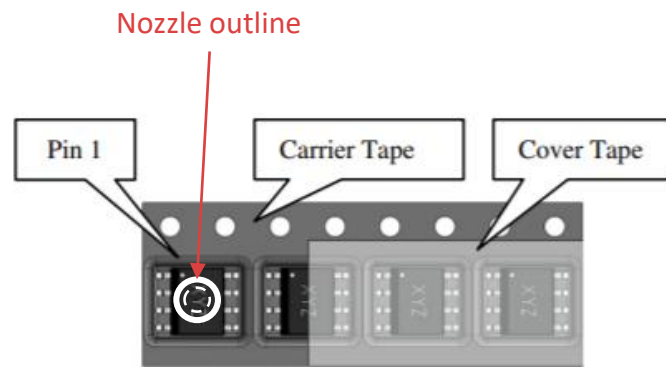
Method of Pick-&-Place (PnP) by package family



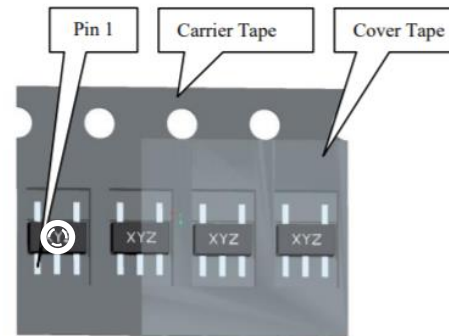
Universal nozzle (needle) is not recommended because of the small contact area with the top surface of the mold

3.2 Component placement

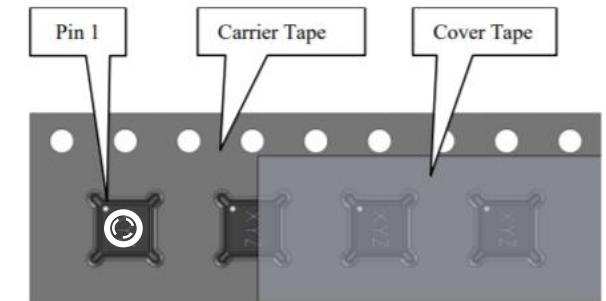
Device delivery in embossed tape on reel (TOR)



Example of SOIC8
(Gull wing package family)



Example of SOT25
(Straight leads package family)



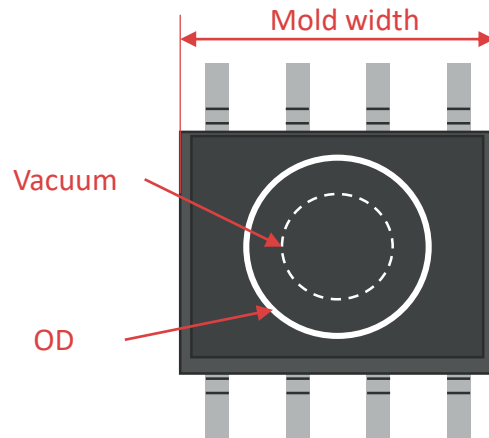
Example of QFN
(BTC package family)

Embossed tape on reel is according to IEC 60286-3. Contact Melexis for the TOR specification of a particular package.

Some ICs have the option to be taped face up or face down, which is indicated by a separate product option code. Refer to the datasheet of the product for more information.

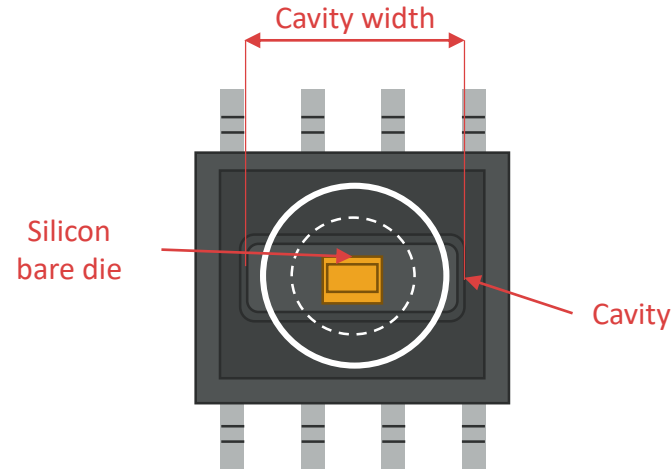
3.2 Component placement

Nozzle selection guidelines



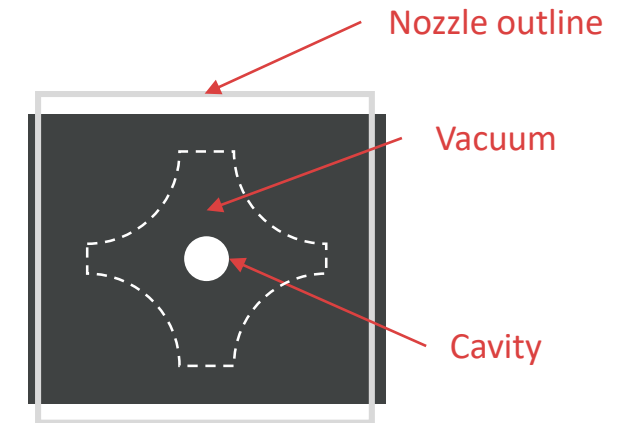
Example of circular nozzle for SOIC8

Outside diameter (OD) of nozzle should be > 50% of mold width



Example of circular nozzle for SOIC8 optical sensor

Outside diameter (OD) = 2*width of optical cavity



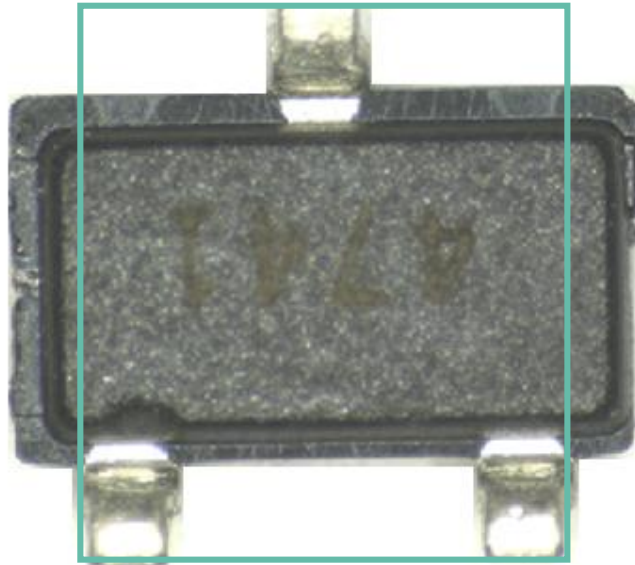
Example of rectangular nozzle for QFN/DFN pressure sensor package

Landing of nozzle should be on the whole package and should not apply force on the center of the package

Some packages in the gull wing and BTC families have a cavity for specific applications. In these, the **bare silicon die active surface is exposed and it can be damaged easily if there is physical contact between the nozzle and the die.** Therefore, nozzle landing shall be on the mold body and not inside the cavity. Rubber nozzle is not allowed. Only metal, ceramic or hard plastic nozzle with flat landing area are allowed.

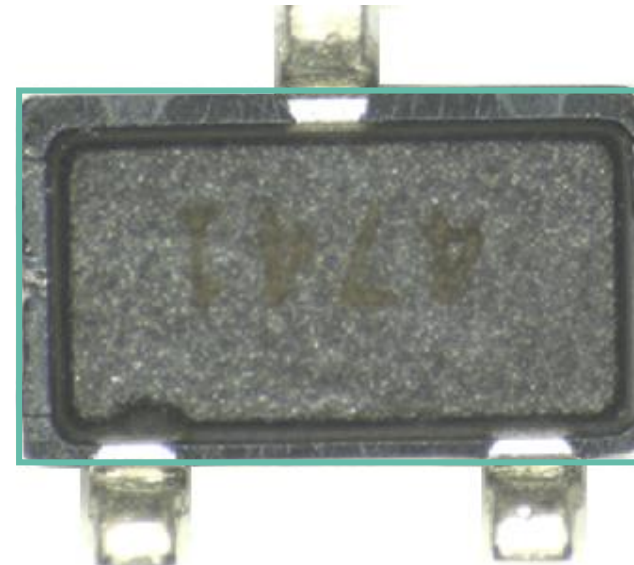
3.2 Component placement

Component outline capture by camera



ALIGNMENT BY PIN OUTLINE

Position error is 100 um



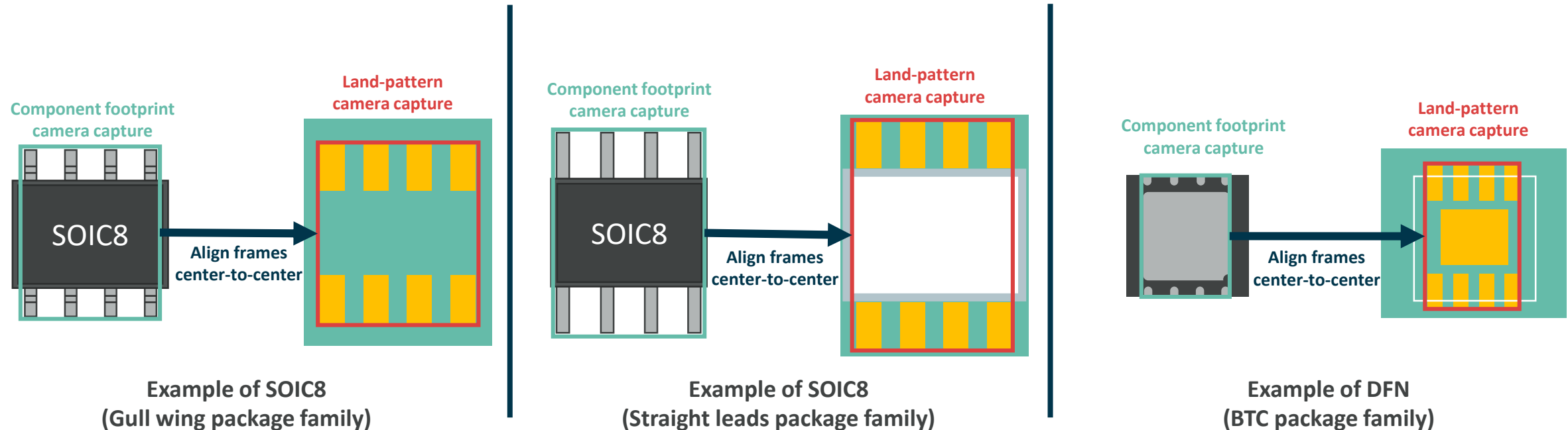
ALIGNMENT BY MOLD OUTLINE

Presence of mold flash adds a non-predictable error of 150um

If PnP alignment camera captures the device mold package, mold flash will create an off-center error up to 0.15mm in X and/or Y. As mold flash varies from chip to chip, offset error will vary accordingly.

3.2 Component placement

Alignment method of SMD package to PCB solder pad

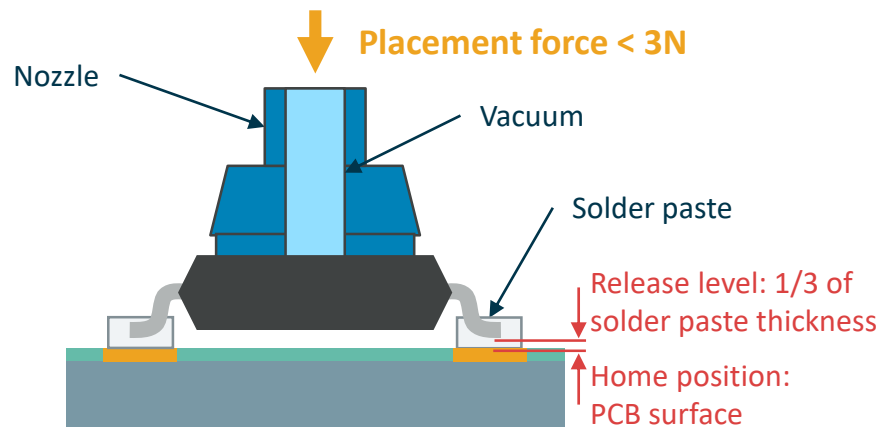


It is recommended to align optically the component by pin outline to the PCB solder pad outline. The PnP alignment camera can capture the outline from the bottom for the components, and from the top for the PCB.

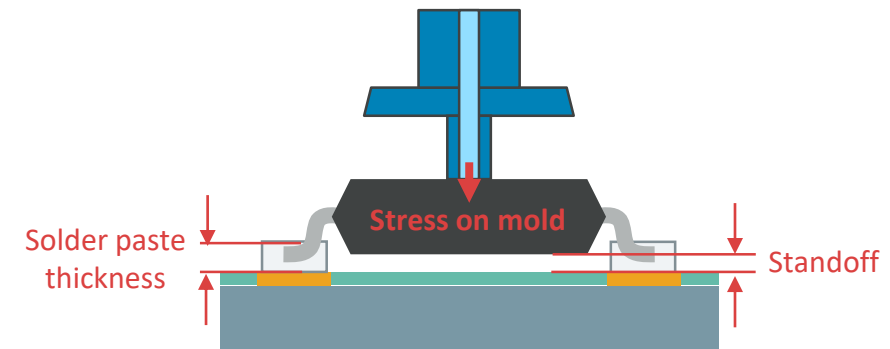
Alignment of QFN/DFN to PCB should be done taking the bottom image of the QFN/DFN pad, not the silhouette of the QFN/DFN mold package.

3.2 Component placement

Placement of gull wing packages onto PCB by nozzle



Example with circular nozzle
RECOMMENDED



Example with universal nozzle
NOT RECOMMENDED

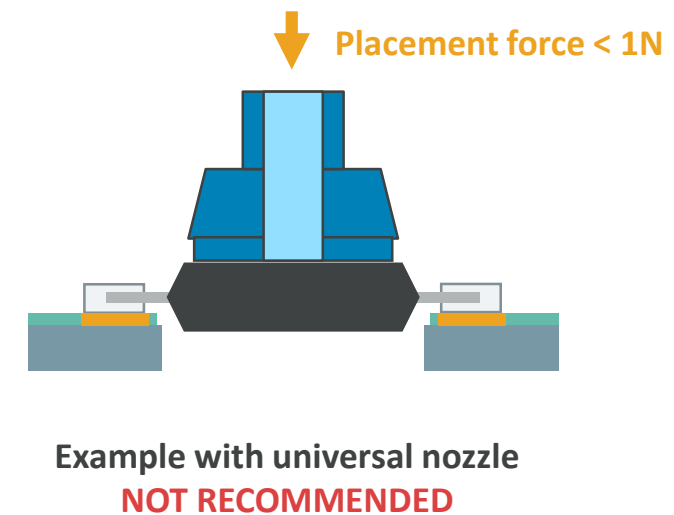
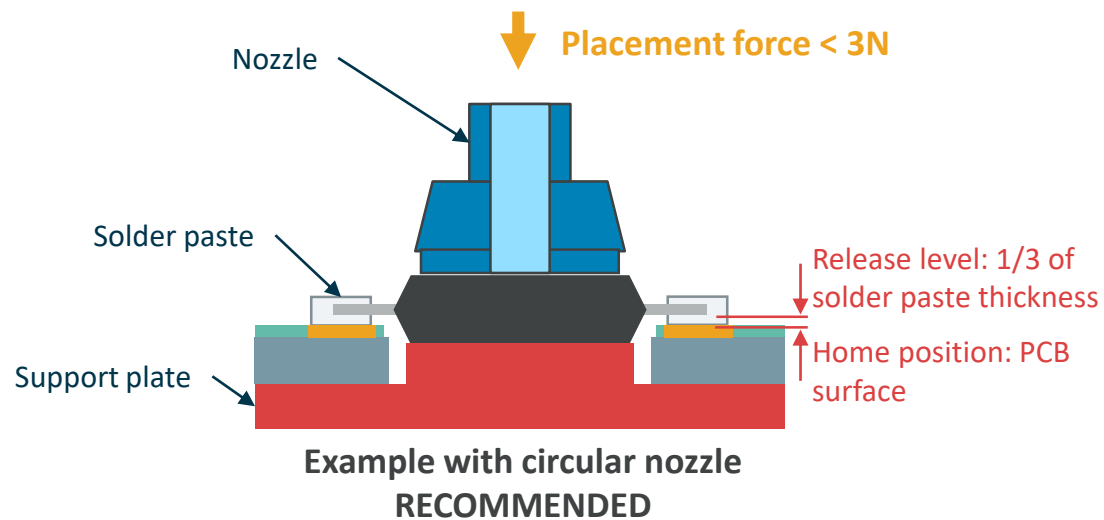
Universal nozzle (needle) is creating a bending stress on the middle of the mold body, while the pins are supporting it from the sides. The plastic deformation becomes more pronounced with small pin count devices, like SOT23: the standoff can be up to 250 μm , which gives lots of space for Z displacement. Hence universal nozzle is not recommended

If the placement force is bigger than 3N, it might deform the leads in such a way that they stretch over the solder pads. Plastic deformation might lead to mold crack at the pin shoulder, as well as delamination of pin-to-mold interface.

Coplanarity of gull wing packages is specified in standard MS-012 and MS-013 as a maximum of 100 μm , which for a solder paste of 150 μm is enough to guarantee contact. Hence, the maximum non-linearity of the PCB panel should be kept to less than 50 μm

3.2 Component placement

Placement of straight leads packages onto PCB by nozzle

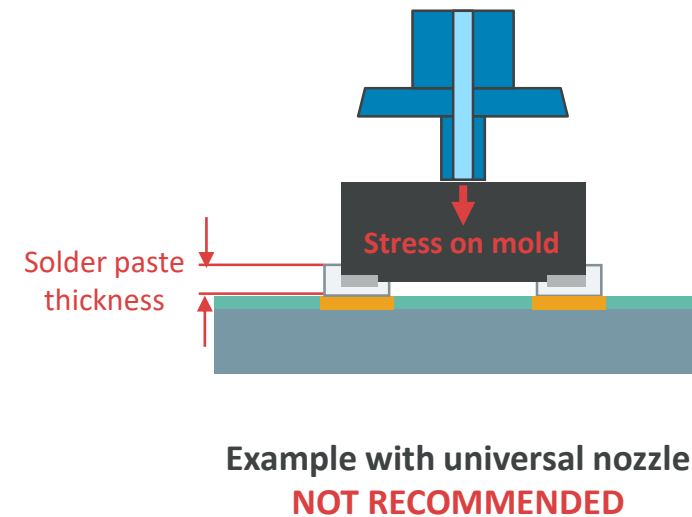
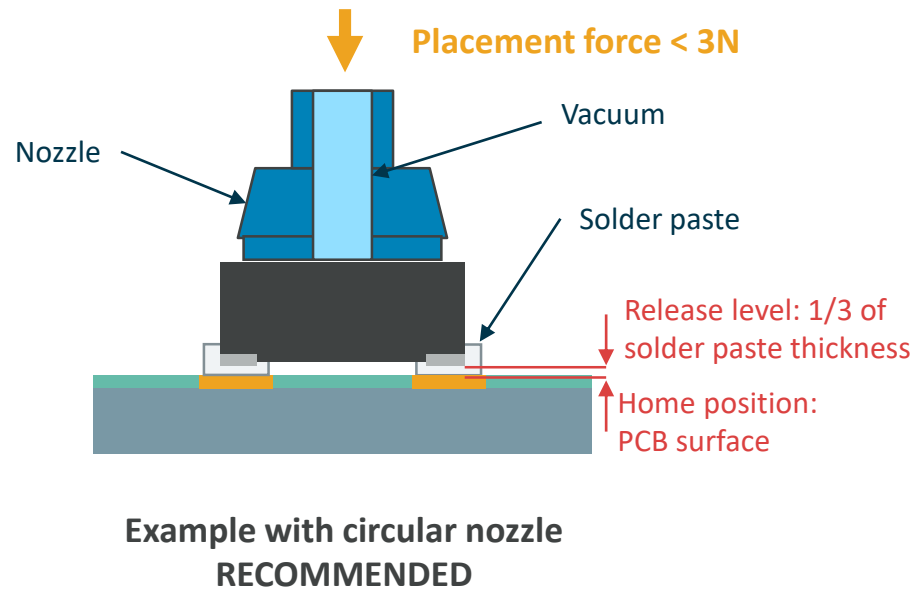


During placement of straight leads packages, there might be a bending stress on the pins by lever effect if the Z release position is not properly controlled. This might lead to delamination in the interface pin-mold and mold crack. It is **strongly recommended** to use a support plate during component placement. The support plate should be planarized with the PCB to make sure the IC is not pushed out.

If the force is limited to <1N with a real-time force control, the support plate it is not needed.

3.2 Component placement

Placement of BTC packages onto PCB by nozzle

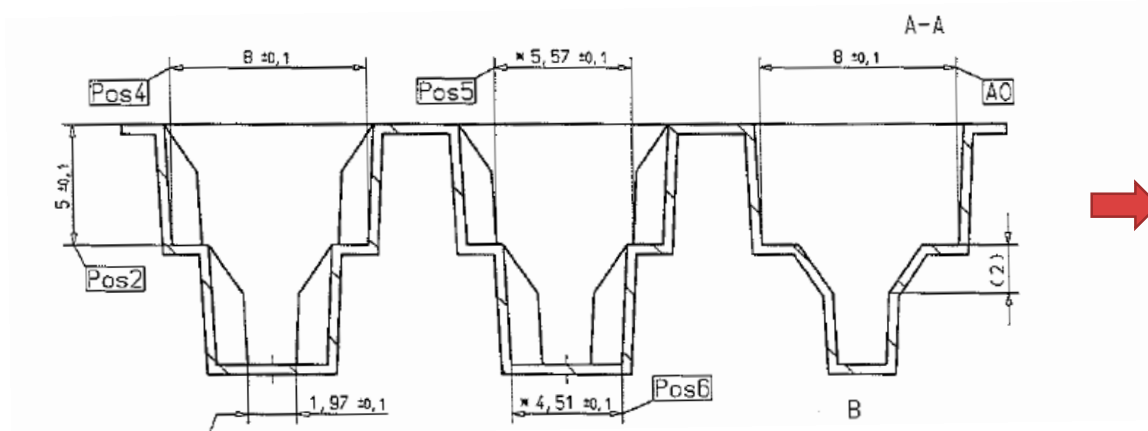


BTC packages have a thin mold body, so it is recommended to use force control placement on PCB. The stress of PnP machine is transferred directly to the die through the mold body. It is recommended to use a nozzle with the greatest contact area to mold body possible.

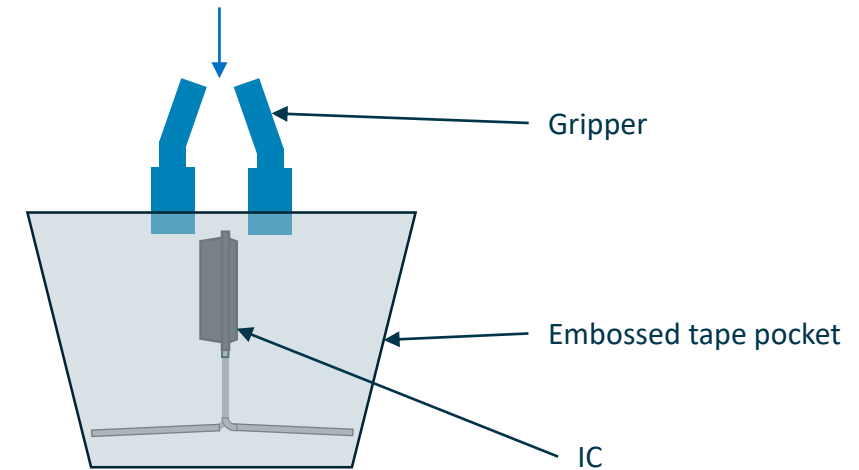
If possible, force shall be distributed on a large surface of the package to reduce the risk of mechanical damage.

3.2 Component placement

Device delivery in embossed tape on reel for SIP in SMD shape



Example of embossed tape on reel with pockets



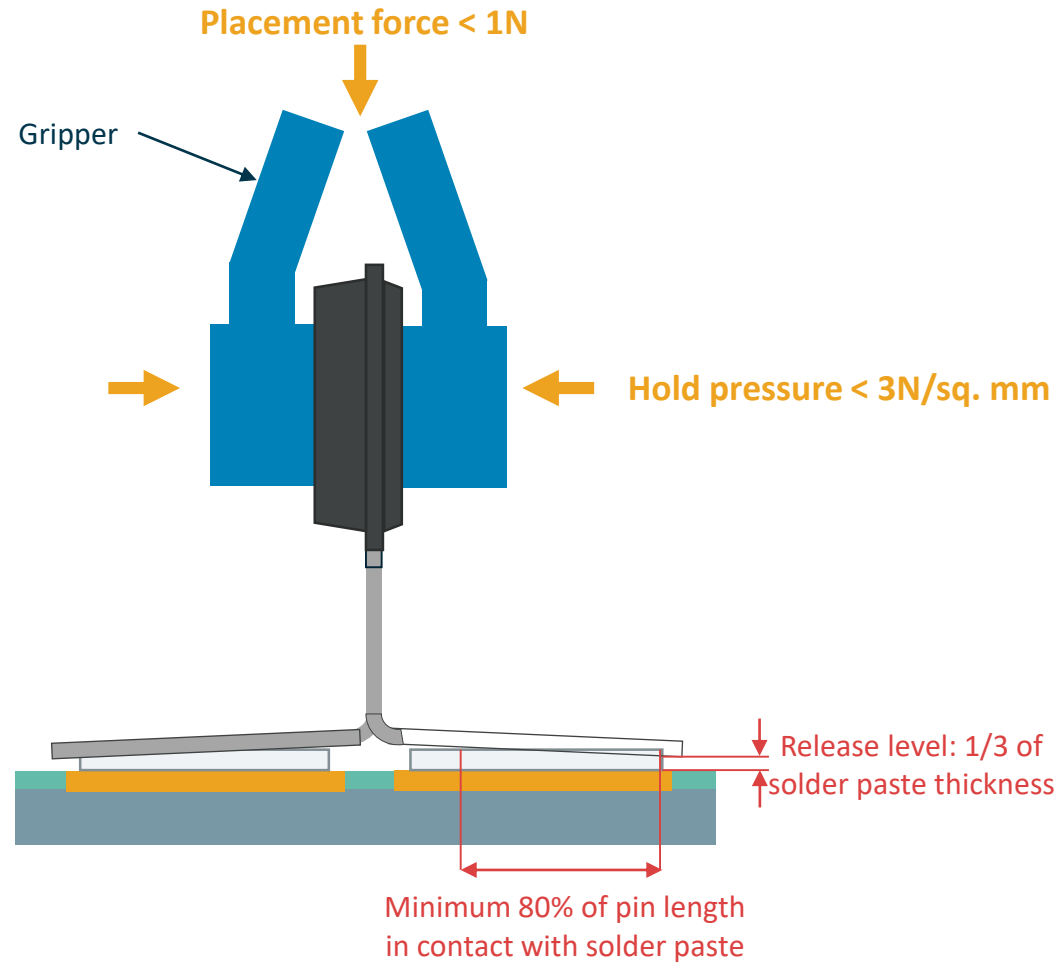
Example of nozzle gripper accessing pocket

Embossed tape on reel for SIP in SMD shape is custom made. Contact Melexis for the TOR (Tape On Reel) specification.

The nozzle gripper should be small enough to enter the pocket where the IC is placed.

3.2 Component placement

Placement of SIP packages in SMD shape onto PCB by gripper



Exceeding the placement force might lead to extra bending of the leads and springback effect.

Exceeding the hold pressure of the gripper on the mold body might lead to mechanical damage of the package.

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3.4 Solder joint inspection & rework

3.3 Reflow soldering

Air/Nitrogen convection reflow oven

Convection reflow oven recommendations from Melexis ICs point of view

Number of zones

8 zones minimum for a lead-free process

6 zones minimum for a SnPb process

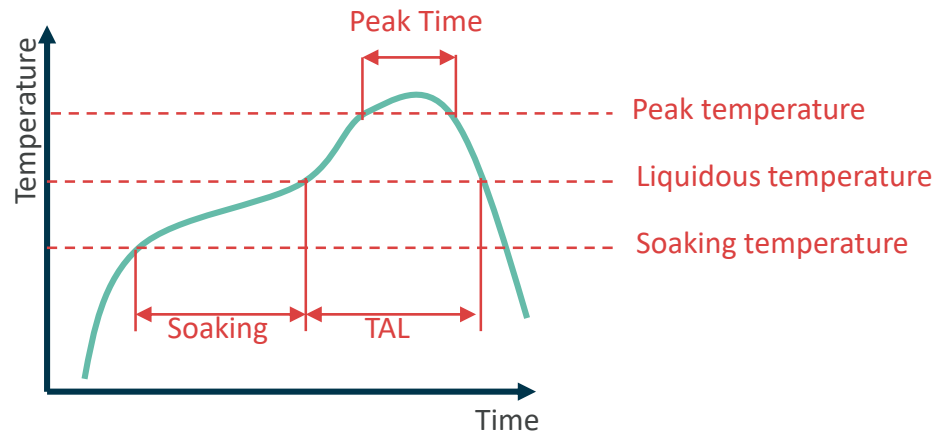
Size of reflow oven and heat zone length

It should be chosen in relation to the PCB panel size

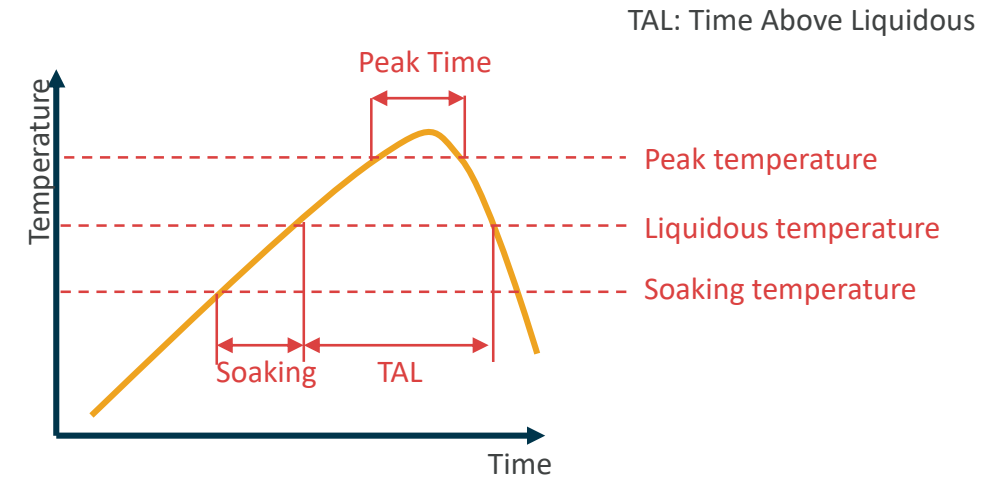
It is strongly recommended to use a nitrogen convection reflow oven, to avoid further oxidation of the leads and PCB during the reflow process: oxidation might lead to voids in the solder joint and failure in the field due to thermal cycling.

3.3 Reflow soldering

Considerations in profile features



Shoulder type profile



Linear type profile

Both shoulder and linear type profiles are applicable to Melexis components, it depends on the other components, as well as the PCB structure and size.

- **Soaking time:** It makes sure that the flux is activated and deoxidizes the solder grains and PCB pad finish.
- **Time above liquidous :** It secures the melting of the solder.
- **Peak time:** It allows for wetting of solder to PCB pad and component leads and IMC (intermetallic compound) formation.

3.3 Reflow soldering

Classification profile for product MSL qualification

Melexis uses reflow profiles in product/package qualification testing and MSL qualification, as defined in the standard *“Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices”* (J-STD-020). Melexis products are qualified for a maximum of 3 times reflow process in a sequence with parameters specified in the *“Table 5.2 - Classification Profiles”* of the J-STD-020E standard where the classification temperature $T_c = 260^\circ\text{C}$. This reflow profile is for classification/preconditioning and is not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in the table below:

Peak temperature: 260 °C	Peak temperature duration: 30 seconds	Temperature ramp-up rate: 3 °C/second max.	Temperature ramp-down rate: 6 °C/second max.	Time 25 °C to peak temperature: 8 minutes max.
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Development of actual reflow soldering profile and parameters at customer should follow the standard *“Requirements for soldered electrical and electronic assembly”* (J-STD-001). It has to be verified that temperature measured on the center of the package does not exceed the limit values of the classification profile given above. Resulting soldering quality for all onboard components has to meet the acceptance criteria defined in the standard *“Acceptability of Electronic Assemblies”* (IPC-A-610).

Melexis does not recommend reflow profiles: the classification profile is just for moisture sensitivity qualification purposes

3.3 Reflow soldering

Flux washing

When using No-clean, Halogen Free solder paste/flux, washing is not needed. For QFN/DFN components only No-clean, Halogen Free flux shall be applied

If a water-soluble flux is used, washing is a must, according to the supplier instructions.

Ultrasonic bath is not recommended since the vibration energy might damage the solder joint or even the component itself. This is specially true for straight lead packages because they are not supported on the bottom.

If above recommendations can not be met, contact Melexis to find a solution.

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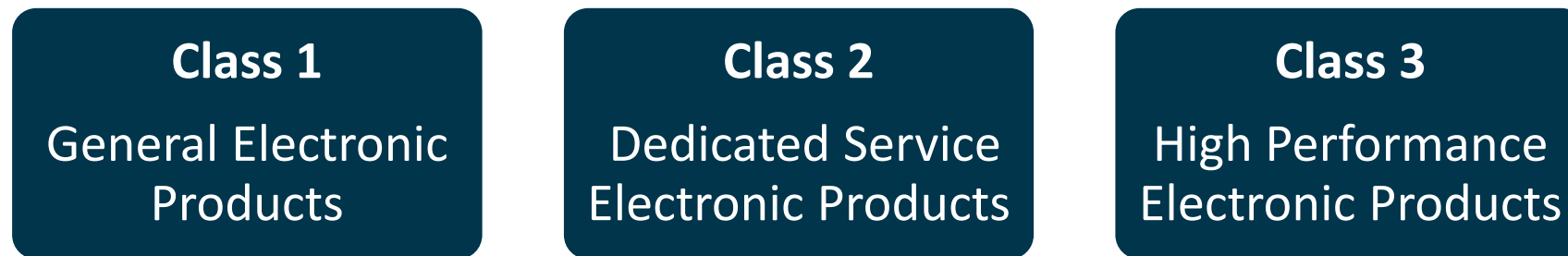
3.3 Reflow soldering

3.4 Solder joint inspection & rework

3.4 Solder joint inspection & rework

Solder joint inspection

The soldering quality acceptance criteria are defined in IPC-610 standard for three different classes of products:

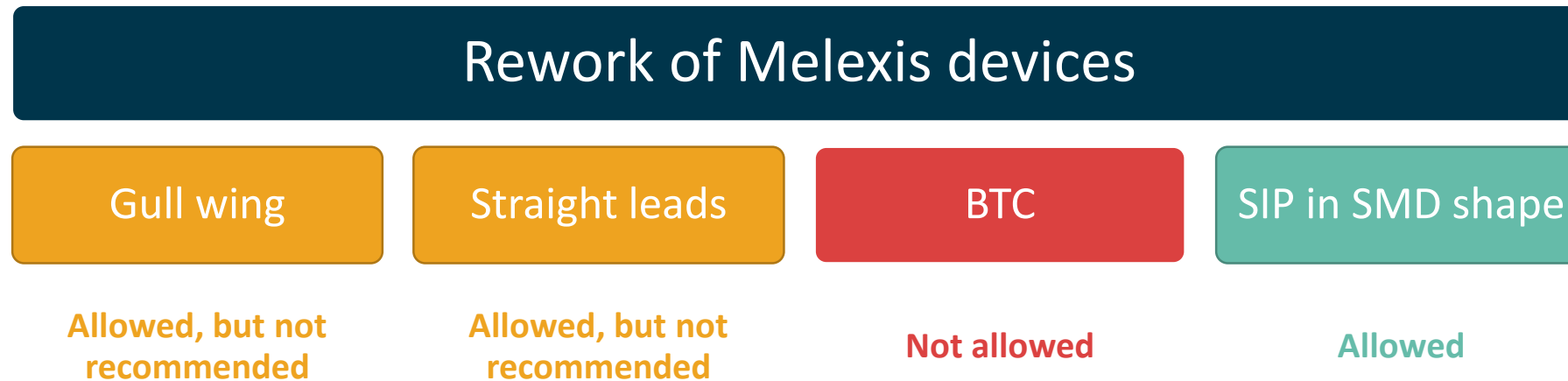


These criteria can be introduced in the AOI system to detect good from bad solder joint, using a reference device.

For BTC packages, it is recommended to apply X-ray inspection of bottom solder joints (AXI).

3.4 Solder joint inspection & rework

Rework



Rework should be done according to standard IPC-7711C/7721C *Rework, Modification and Repair of Electronic Assemblies*

SIP packages in SMD shape can be re-soldered using manual or robot soldering iron, limited to **350C for 10sec or 380 degC for 5 seconds.**

Important: The flux inside the solder wire used for re-soldering shall be No-clean, Halogen Free.

For SMD and straight leads, contact Melexis for an assessment.

Annex I: List of Abbreviations

AOI: Automatic Optical Inspection

AN: Application Note

AXI: Automatic X-Ray Inspection

BGA: Ball Grid Array

BTC: Bottom Terminated Component

DFN: Dual Flat No-Leads

ENEPIG: Electroless Nickel/Electroless Palladium/Immersion Gold

ENIG: Electroless Nickel Immersion Gold

HASL: Hot Air Solder Leveling

IC: Integrated Circuit

IMC: Intermetallic Compound

Imm Ag: Immersion Silver

Imm Sn: Immersion Tin

LF HASL: Lead-Free Hot Air Solder Leveling

MSL: Moisture Sensitivity Level

NB: Narrow Body

NiPdAu: Nickel-Palladium-Gold

NSMD: Non Solder Mask Defined

OSP: Organic Solderability Preservative

PCB: Printed Circuit Board

PnP: Pick and Place

POD: Product Outline Drawing

PQR: Product Qualification Report

QFN: Quad Flat No-Leads

QFP: Quad Flat Package

SIP: Single Inline Package

SPI: Solder Print Inspection

SM: Solder Mask

SMD: Solder Mask Defined

SMD: Surface Mount Device

SMT: Surface Mount Technology

Sn: Tin

SnPb: Tin-Lead

SOIC: Small Outline Integrated Circuit

SOT: Small Outline Transistor

SPI: Solder Paste Inspection

SSOP: Thin Shrink-Small Outline Package

TAL: Time Above Liquidous

Tc: Classification Temperature

THD: Through-Hole Device

TOR: Tape On Reel

TSSOP: Thin Shrink-Small Outline Package

UTDFN: Ultra Thin Dual Flat No-Leads

WB: Wide Body

Xc, Yc, Zc: Magnetic center in X, Y and Z dimensions

Annex II: List of Standards

J-STD-001: Requirements for Soldered Electrical and Electronic Assemblies

J-STD-002: Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-004: Requirements for Soldering Fluxes

J-STD-005: Requirements for Soldering Pastes

J-STD-020: Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices

J-STD-033: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

MS-012: Plastic Dual Small Outline Gull Wing 1.27mm Pitch Package

MS-013: Very Thick Profile, Plastic Small Outline Family, 1.27 mm Pitch, 7.50 mm Body Width

JESD22-A113H: Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

EN60068-2-20: Test methods for solderability and resistance to soldering heat of devices with leads

IPC-A-610: Acceptability of Electronic Assemblies

IPC 2221: Generic Standard on Printed Board Design

IPC-7351: Generic Requirements for Surface Mount Design and Land Pattern Standard

IPC-7525: Stencil Design Guidelines

IPC-7711C/7721C: Rework, Modification and Repair of Electronic Assemblies

IEC 60286-3: Packaging of Surface Mount Components on Continuous Tapes

IEC 60749-15: Resistance to Soldering Temperature for Through-hole Mounted Devices

Annex III: List of Application Notes

Guidelines for lead forming of Hall sensors in SIP package

Guidelines for storage and handling of plastic encapsulated ICs



Melexis

INSPIRED ENGINEERING

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