MLX90514 - Robotics and Industrial

Dual Input Inductive Position sensor interface IC
Datasheet

General description

Features and benefits

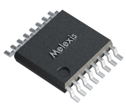
- High resolution inductive encoder with synchronized dual input channel readout
- On-chip Vernier angle calculation with 16-bit resolution
- High accuracy: maximum error $\pm0.36\,°$electrical for each inductive channel
- 16-point programmable linearization characteristic per input channel
- Immune to magnetic stray fields (ISO 11452-8)
- < 1 µs latency thanks to on-chip propagation delay compensation
- On-chip signal processing for enhanced accuracy and excellent dynamic behavior
- SPI or SSI output with wide frame content flexibility
- Ambient Operating Temperature Range from -40 °C to 125 °C
- TSSOP-16 Package RoHS Compliant
- Facilitates compliance with safety standards up to SIL 2

Description

The MLX90514 is a dual input inductive encoder suitable for robotic and industrial applications where the simultaneous measurement of two positions is required. The position information derived from the two channels can be directly transferred to the output or used for the calculation of a 16-bit Vernier angle.

The MLX90514 is designed to control an inductive sensor system formed by the transmitting coil, one or multiple targets and two sets of receiver coils, each composed of three receiver coils. The on-chip LC oscillator generates an electromagnetic field together with the transmitting coil. This electromagnetic field induces, via the target(s), angle dependent voltages in the receiving coils. These signals are captured and processed by the MLX90514 internal DSP units according to the device configuration.

The MLX90514 offers multiple output modes. An SPI protocol allows fast protected data transfer and device programming. The SSI enables fast data output with a 2-wire connection.



TSSOP-16

Application examples

- High resolution rotary sensor
- High resolution linear sensor

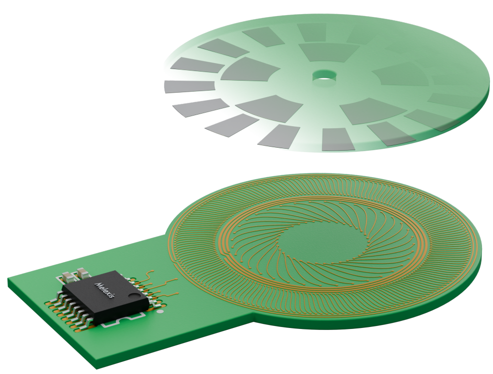


Figure 1: Rotary encoder application example

Contents

1 Ordering information

Ordering Code	Temperature	Package	Definition	Packing
MLX90514KGO-AAA-150-RE	-40 °C to 125 °C	TSSOP-16	SPI/SSI output mode	Reel

Table 1: Ordering codes

2 Glossary of terms

Term	Description
°el / °mech	Electrical / mechanical degree : °el = °mech · sensor periodicity
ABE	Analog Back-end
ADC	Analog-to-Digital converter
AGC	Automated gain control
AFE	Analog Front-end
AoU	Assumptions-of-Use
SIL	Safety Integrity Level
CDM	Charge Device Model
CMRR	Common Mode Rejection Ratio
DAC	Digital-to-Analog Converter
DC	Direct Current
DSP	Digital Signal Processing
EEPROM	Electrically Erasable Programmable Read Only Memory
ECU	Electronic Control Unit
EMC	Electro-Magnetic Compatibility
e-rpm	Electrical Revolutions per Minute. 1 e-rpm = 6 °el/s
ESD	Electro-Static Discharge
FDTI	Fault Detection Time Interval
FHTI	Fault Handling Time Interval
GND	Ground
HBM	Human Body Model
Hi-Z	High Impedance
I/O	Input / Output
ISO	International Standardization Organization
LC	Inductor-Capacitor
LCO	LC Oscillator
LSB	Least Significant Bit
MISO	Master-In Slave-Out
MOSI	Master-Out Slave-In
PA	Primary angle

Term	Description
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PGI	Programming Interface
POR	Power-On Reset
PTC	Programming-Through-Connector : Melexis programming tool via PGI
RCO	RC Oscillator
rpm	Rotation per minute
Rx	Receiver
SA	Secondary angle
SAD	Set Circuit Address
SEooC	Safety Element Out-of-Context
SPI	Serial Peripheral Interface
TDMA	Time Division Multiple Access
TSSOP	Thin-Shrink Small-Outline Package
T_A	Ambient temperature
Tx	Transmitter
VA	Vernier angle
VDP	Vernier divider primary
VDS	Vernier divider secondary
VM	Vernier multiplier
V_P	Peak voltage
$V_{SE,pp}$	Single-ended peak to peak voltage

Table 2: Glossary of terms

3 Marking, pin definitions and descriptions

For more information see application diagrams in Section 12.

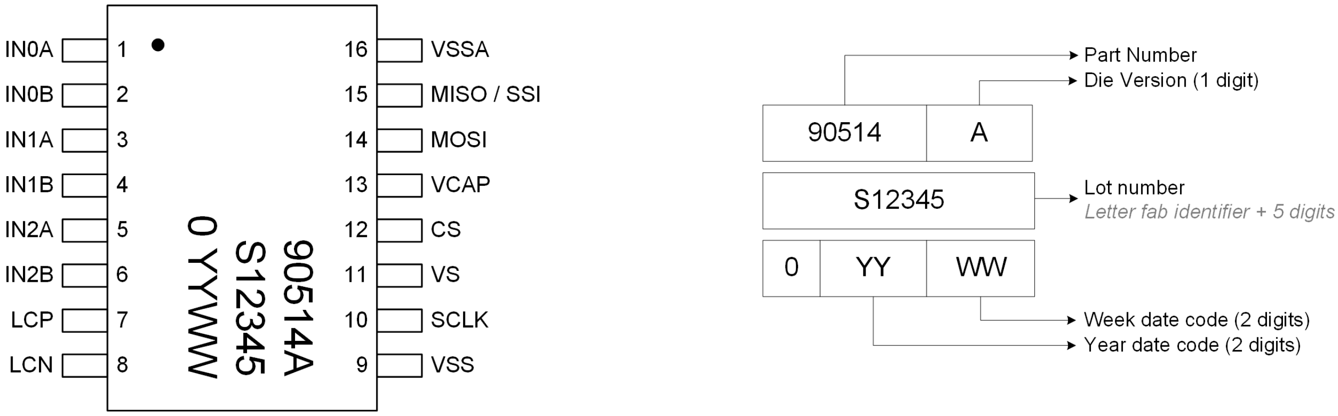


Figure 2: TSSOP-16 pin names and marking

Pin	Name	I/O type	Description
1	IN0A	I	Sensor receiver coil signal input 0, channel A
2	IN0B	I	Sensor receiver coil signal input 0, channel B
3	IN1A	I	Sensor receiver coil signal input 1, channel A
4	IN1B	I	Sensor receiver coil signal input 1, channel B
5	IN2A	I	Sensor receiver coil signal input 2, channel A
6	IN2B	I	Sensor receiver coil signal input 2, channel B
7	LCP	O	Transmitter coil, positive connection
8	LCN	O	Transmitter coil, negative connection
9	VSS	Ground	Digital, LCO and output driver ground
10	SCLK	I	SPI or SSI serial clock input
11	VS	Power	Power supply voltage
12	CS	I	SPI - CS (chip select)
13	VCAP	Power	External supply buffer capacitor connection
14	MOSI	I	SPI - MOSI
15	MISO	O	SPI - MISO / SSI - DATA
16	VSSA	Ground	Analog ground

Table 3: TSSOP-16 pin definition and description

4 Absolute Maximum Ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Ambient temperature	T_A	-40		125	°C	
Junction temperature	T_{JUNC}			135	°C	
Storage temperature	$T_{STORAGE}$	-55		175	°C	
Supply voltage	VS	-6		6	V	Continuous
ESD CDM robustness	V_{CDM}			±500	V	All pins, according to AEC-Q100-011
	V_{CDM}			±750	V	Package corner pins
	V_{HBM}			±2	kV	All pins
Pin voltage range INx	V_{INx}	-0.3		5.5	V	
Pin voltage range LCP, LCN	V_{LCN}/V_{LCP}	-2.0		5.5	V	
Pin voltage range GPIOs	V_{GPIO}	-0.3		5.5	V	GPIO: CS, SCLK, MOSI, MISO
Pin voltage range VSSA, VSS	VSSA/VSS	-0.3		0.3	V	

Table 4: Absolute maximum ratings

5 General electrical specifications

MLX90514 Electrical Specifications are given in Table 5.

T_A = -40 °C to 125 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Position signal accuracy [1]	$Acc_{position}$	-0.36		0.36	°el	Applies to φ_{DLCA}, φ_{DLCB}
Position signal rms noise [2]			0.025		°el	LFC = 0, 1, 2
			0.035		°el	LFC = 3, 4
			0.055		°el	LFC = 5
			0.075		°el	LFC = 6
			0.100		°el	LFC = 7
Supply current operation	I_{VS}			12	mA	LCO disabled, No MISO load, f_{AC} ≤ 10 MHz
	I_{VS}			20	mA	LCO: Q = 18, f_{AC} ≤ 20 MHz
Inrush current	$I_{VS\_startup}$		50	100	mA	C_{VS} = C_{VCAP} = 470 nF, VS rise time > 100us
Thermal resistance - junction to ambient	R_{thja}			99	K/W	
Thermal resistance - junction to case	R_{thjc}			27	K/W	
Supply Voltage	VS	4.5	5.0	5.5	V	
Input low voltage	V_{IL}			0.3	VCAP	MOSI, CS, SCLK
Input high voltage	V_{IH}	0.7			VCAP	MOSI, CS, SCLK
Output low voltage	V_{OL}			0.4	V	MISO
Output high voltage	V_{OH}	0.8			VCAP	MISO
Output driver strength	$I_{O\_H/L}$	16			mA	MISO
VS POR voltage IC OFF	VPORB_HL	1.50	1.85	2.00	V	
VS POR voltage IC ON	VPORB_LH	2.05	2.45	2.70	V	
EEPROM programming temperature	T_{EEPROM}	-40		125	°C	
EEPROM erase/write cycles				600		per row and column

Table 5: Electrical and system level performance specification

[1] The value reported is a ±3σ value including noise assuming LFC = 0 settings and delay compensation. The value reported is valid within the speed and acceleration ranges detailed in see Section 7.4.1, and

with ideal, offset free input signals. For errors related to the input signal offset compensation, refer to Section 7.5.1.

[2] The value refers to room temperature.

6 Timing specification

6.1 General timing Specifications

Operating Characteristics, VS = 4.5 V to 5.5 V, T_A = -40 °C to 125 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
LCO start-up time	$T_{startup\_LCO}$		20	100	µs	
RC oscillator frequency	f_{RCO}	19.3	20	20.7	MHz	Factory trimmed
Application clock	f_{AC}	$f_{RCO}/4$		f_{RCO}	MHz	
Latency	$\Delta\tau_{phi}$	-1		1	µs	With delay compensation
Initialization time [1]	T_{INIT}	0.5	0.7	0.9	ms	f_{AC} = 20 MHz
Start-up time [1]	T_{STUP}	0.7 2.8 11.1	1.0 2.9 11.2	2 [2] 3.0 11.5	ms ms ms	MUPET_CAP = 3 MUPET_CAP = 1 MUPET_CAP = 0

Table 6: General timing parameters

[1] VS rise time from 0 V to 5 V in 100 µs.

[2] DSP_LFC_HI $\geq$ 5, f_{AC} = 20 MHz

The application clock frequency f_{AC} is controllable by field AC_SEL [2:0] with following mapping:

AC_SEL	f_{AC} [MHz] (typ.)
3	10
5	5
0 (default)	20

Table 7: Application clock frequency f_{AC} programming

A lower application clock reduces the MLX90514 current consumption for digital signal processing and ADC but comes with restrictions on dynamic characteristics and communication speed.

6.2 Startup time

The startup time T_{STUP}, see Table 6 is the duration between power-on reset (POR) until the output interfaces are enabled and the internal angular acquisition has finished. During this period the pin SCLK should not be activated.

With enabled cold activation of the MUPET programming interface (MUPET_CAP $\neq$ 3) pin OUT stays in Hi-Z until T_{STUP} independent from acquisition procedure of the angular data, see Table 6. This in turn delays all communication on SPI and SSI accordingly.

Without MUPET cold activation (MUPET_CAP = 3) T_{STUP} is the sum of T_{INIT} and a period for the DSP angular acquisition. While the output interfaces are enabled after T_{INIT} they report safe state until the DSP confirms valid angular data.

For all communication interfaces during startup the sensor reports safe state SS2 (Hi-Z) or SS3, see Section 10.3.

7 Detailed description

7.1 Block diagram

The MLX90514 is an inductive position sensor which is used for absolute rotary or linear motion/position sensing (defined by the coil system). In Figure 3 the block diagram is given.

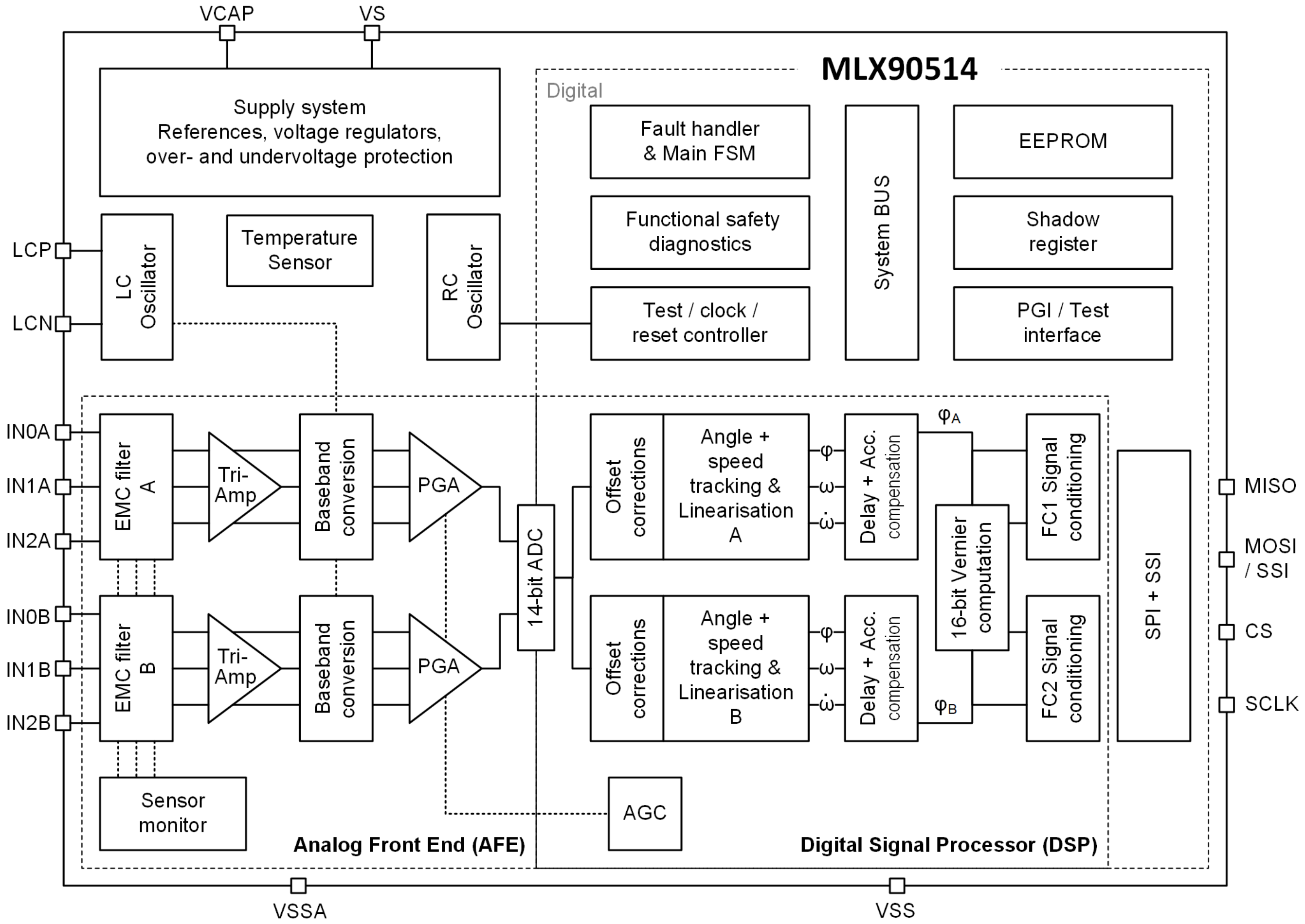


Figure 3: Block diagram

The main functional sections are: sensor excitation with an LC Oscillator (LCO), the Analog Front-end (AFE) performing the sensor position signal analog pre-processing, the Analog-To-Digital Conversion (ADC) followed by the Digital Signal Processing (DSP) and the SPI / SSI engine as programming and output interface.

The AFE consists of two channels A and B, each equipped with an EMC filter, Tri-Amplifier, baseband conversion and a Programmable Gain Amplifier (PGA). The digital core provides the signal processing for angular computation and system control as well as the protocol engines for SPI and SSI. The main supporting functionalities are the supply system, functional safety diagnostics, the customer programming interface (PGI) and an EEPROM for the system configuration data storage.

The functional safety concept provides self-diagnostic features to check the integrity of the sensor coil system, the integrity of the input and output signals, and the IC itself.

7.2 Supply system

The MLX90514 has an integrated supply system providing regulated supply and reference voltages, as well as bias currents.

These regulated supply voltages guarantee immunity against disturbances on the external power supply, required for the correct functionality of the sensor IC. The capacitance at the pin VCAP, refer to Section 12, serves as an energy storage during short VS voltage dips.

7.3 Sensor coil system

MLX90514 is designed for an external sensor (coil system) consisting of one transmitting coil (Tx) and two sets of three receiving (Rx) coils each. The parameters described in this section specify the electrical characteristics of the sensor coil system, but do not constitute a full inductive sensor design guideline. For details and support for the sensor and target design please contact the Melexis sales office.

7.3.1 Tx coil and LC oscillator

The LCO drives the Tx coil of the sensor coil system. The LCO frequency (f_{LCO}) is defined by the external inductance (L_{Tx}) and the two external capacitors C_{LCO} (see Figure 4). A customization of the frequency is possible by variation of L_{TX} and C_{LCO}. The R_{TX} represents the internal resistance of the Tx coil.

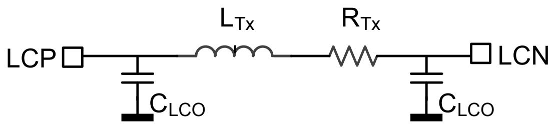


Figure 4: LCO Tx coil model

The LCO frequency can be calculated using the flowing formula:

$$f_{LCO} = \frac{1}{2\pi}\sqrt{\frac{1}{L_{Tx}\cdot(C_{LCO}/2)} - \left(\frac{R_{Tx}}{L_{Tx}}\right)^2}$$

The LCO amplitude can be scaled by setting LC_OSC_AMP to 1. A reduced LCO amplitude is used for cases where the maximum input signal amplitude (A_{Rotor}) is exceeded (refer to Section 7.4.1) or to reduce emissions.

The LCO frequency (f_{LCO}) is defined by the Tx coil inductance (L_{Tx}) and the external capacitors (C_{LCO}). A customization of the frequency is possible by variation of L_{Tx} and C_{LCO}. As an example, for a typical value of f_{LCO} = 2.7 MHz, the external components can be set as L_{Tx} = 4 µH and C_{LCO} = 1.8 nF. However, other component value combinations within the specification range are applicable.

Operating Characteristics, VS = 4.5 V to 5.5 V, T_A = -40 °C to 125 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
LCO frequency range	f_{LCO}	2.0	2.7	5.0	MHz	
LCO common mode voltage	V_{CM}		1.68		V	

Parameter	Symbol	Min	Typ	Max	Unit	Comment
LCO amplitude	A_{LCO}	2.05	2.4	2.7	$V_{SE,pp}$	LC_OSC_AMP = 0
Scaled LCO amplitude	A_{LCO}	1	1.4	1.55	$V_{SE,pp}$	LC_OSC_AMP = 1
Tx coil inductance	L_{Tx}	1	4[1]	10	µH	
Tx coil internal resistance	R_{Tx}		5		Ω	
Capacitor	C_{LCO}		1.8		nF	
Tx quality factor	Q_{Tx}		18[1]			$Q_{TX} = 2\pi \cdot f_{LCO} \cdot L_{Tx} / R_{Tx}$
LCO current consumption	I_{VS_LCO}		3[1]		mA	

Table 8: LCO electrical parameters

[1] See Figure 5 for relation between Q_{Tx} and I_{VS_LCO} (typical conditions)

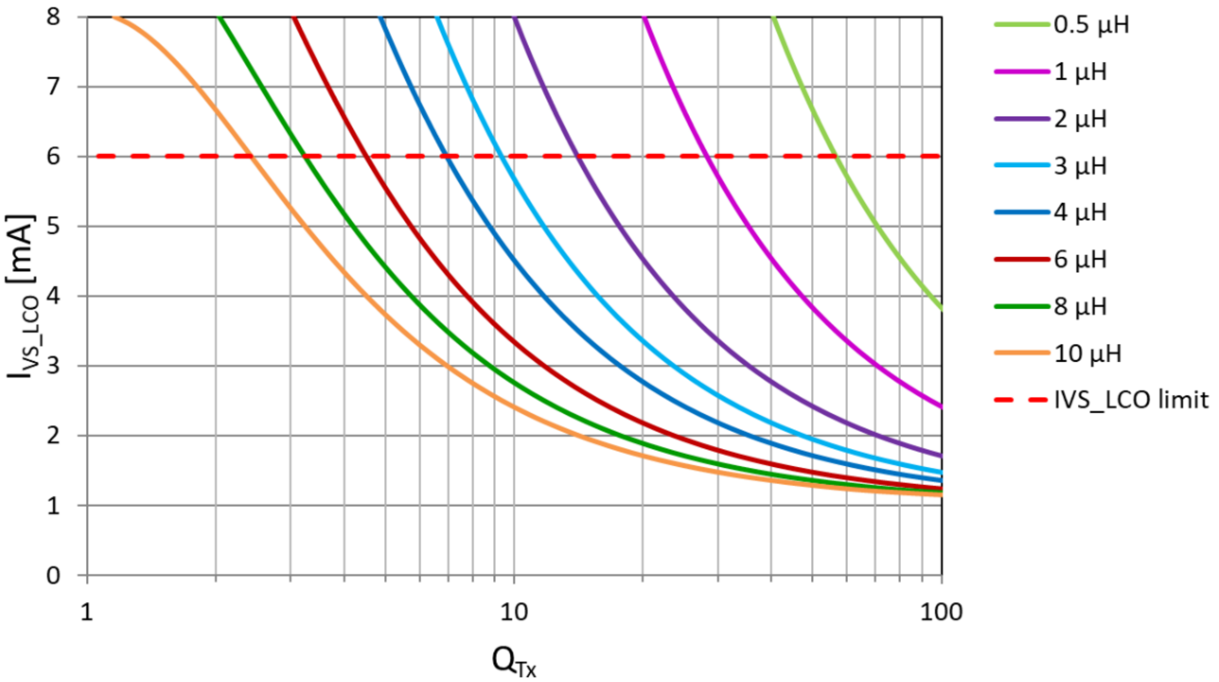


Figure 5: I_{VS_LCO} as function of Q_{TX} for f_{LCO} = 2.7 MHz

7.3.2 Rx coils

The Rx coils electrical specification is given in Table 9. For details and support regarding sensor coil system designs please contact the Melexis sales office.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Rx Inductive component	L_{Rx}	40	200	500	nH	

Table 9: Rx coils specification

Each individual Rx coils set is DC biased by the internal Sensor Bias circuits. Three individual DC operating points per Rx coil set can be chosen by EEPROM register CIDA and CIDB programming for channel A and B, respectively.

For a single sensor module, the default Sensor Bias setting can be used. For a multi-sensor module including more than two sensor coil systems, the DC operating point of the individual sensors must be programmed to different values (CIDA and CIDB setting) for the correct safety function of the sensor short detection.

Operating Characteristics, VS = 4.5 V to 5.5 V, T_A = -40 °C to 125 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Sensor Bias operating point	V_{SOP}	0.66	0.7	0.74	V	CIDA / CIDB = 0 (CIDA default value)
		0.99	1.04	1.09		CIDA / CIDB = 1 (CIDB default value)
		1.35	1.41	1.47		CIDA / CIDB = 2, 3

Table 10: Sensor DC operating points

7.4 Analog signal processing

The transmit coil, excited by the LCO, inductively couples to the two sets of Rx coils corresponding to the A and B channels. The coils are connected to the pins IN0A, IN1A, IN2A and IN0B, IN1B, IN2B, respectively. The strength of the coupling is modulated by the rotor position and leads to amplitude modulated receive signals at LCO frequency.

7.4.1 Input signal specification

The three input signal envelopes from each of the sensor coil sets INxA and INxB are composed of an angular signal of amplitude A_{RotorA} and A_{RotorB}, the common mode level $A_{CommonA}$ and $A_{CommonB}$, and the asymmetry A_{AsymxA} and A_{AsymxB} respectively, according to the formulas below.

$$IN0A, B = A_{RotorA,B} \sin\left(\phi_{A,B} - \frac{1}{6}\pi\right) + A_{CommonA,B} + A_{Asym0A,B}$$
$$IN1A, B = A_{RotorA,B} \sin\left(\phi_{A,B} - \frac{5}{6}\pi\right) + A_{CommonA,B} + A_{Asym1A,B}$$
$$IN2A, B = A_{RotorA,B} \sin\left(\phi_{A,B} - \frac{9}{6}\pi\right) + A_{CommonA,B} + A_{Asym2A,B}$$

$A_{CommonA,B}$ is caused by a common mode direct coupling from the Tx coil into the Rx coils and is equal on all three inputs. The common mode voltage is suppressed by the MLX90514.

$A_{AsymxA,B}$ is caused by the asymmetry of the Rx coils on the PCB. It can have different offset voltages on each INx signal caused by feeding lines from and to the sensor PCB or metal objects close to the PCB sensor. This coil system asymmetry level causes a first-order harmonic on the measured angle and should be compensated using the MLX90514 DC-compensation methods (refer to Section 7.5.1).

Operating Characteristics, VS = 4.5 V to 5.5 V, T_A = -40 °C to 125 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit
INx input signal envelope	A_{RotorA} A_{RotorB}	2.5		100	mV_P
INx common mode amplitude	$A_{CommonA}$ $A_{CommonB}$			min(700 mV, 10 · A_{RotorA}) min(700 mV, 10 · A_{RotorB})	V
INx asymmetry amplitude	A_{AsymA} [1] A_{AsymB} [2]			min(10 mV, 0.7 · A_{RotorA}) min(10 mV, 0.7 · A_{RotorB})	V

Table 11: Input signal requirements

[1] $A_{AsymA} = max(|Asym0A|, |Asym1A|, |Asym2A|)$

[2] $A_{AsymB} = max(|Asym0B|, |Asym1B|, |Asym2B|)$

The maximum input signals frequency (angular speed) is given in Table 12.

Operating Characteristics, VS = 4.5 V to 5.5 V, T_A = -40 °C to 125 °C (unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Electrical angular speed	v_{el}	-240 000 [1]		240 000 [1]	e-rpm	f_{AC} = 20 MHz

Table 12: Electrical rotational speed

[1] If f_{AC} < 20 MHz, this value should be rescaled by a factor f_{AC} [MHz] / 20. It is recommended to consider as well the Nyquist criteria

The maximum input signals frequency variation (angular acceleration) depends on the bandwidth of the phase tracking loop (refer to Section 7.5.2), which is controlled by the LFC parameter as listed in Table 13. The LFC parameter is automatically adapted by the system on the basis of the measured acceleration. The user can restrict the LFC lower and upper bounds via the fields DSP_LFC_LO [2:0] and DSP_LFC_HI [2:0], respectively. Note that Table 13 refers to an application clock f_{AC} = 20 MHz. For other values, the acceleration limits should be scaled by a factor $(f_{AC}\ [MHz]/20)^2$.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Electrical angular acceleration	a_{el}	-18 750		18 750	e-rpm/s	LFC = 0
		-75 000		75 000		LFC = 1
		-300 000		300 000		LFC = 2
		-1 200 000		1 200 000		LFC = 3

Parameter	Symbol	Min	Typ	Max	Unit	Comment
		-4 800 000		4 800 000		LFC = 4
		-19 200 000		19 200 000		LFC = 5

Table 13: Electrical rotation acceleration with f_{AC} = 20 MHz, DSP_SROS = 2

7.4.2 Filtering, amplification and rectification

The input signals INxA and INxB are filtered through the EMC filter to suppress high frequency noise. The common mode of the input signals voltage, caused by symmetrical coupling from the Tx coil, is suppressed by a differential amplifier stage.

The rectifier and low pass filter blocks perform a rectification of the amplifier output signals. The rectification is based on the clock derived from the LCO.

7.4.3 Automatic Gain Control

The rectified signals are subject to an amplification step before being converted to digital signals by the ADC block. The MLX90514 has an automatic gain control (AGC) with 5 gain settings operating independently on channel A and B. The fields AGC_GAIN_MIN [2:0] and AGC_GAIN_MAX [2:0] allow to restrict the AGC dynamic range or even to lock it by programming AGC_GAIN_MIN = AGC_GAIN_MAX. Restricting the AGC range is not recommended and may result in a reduced range for A_{Rotor} as shown in Figure 6, however the self-monitoring of the AGC operation is not affected. The currently selected AGC gain is reported with registers AGC_GAIN_A and AGC_GAIN_B respectively.

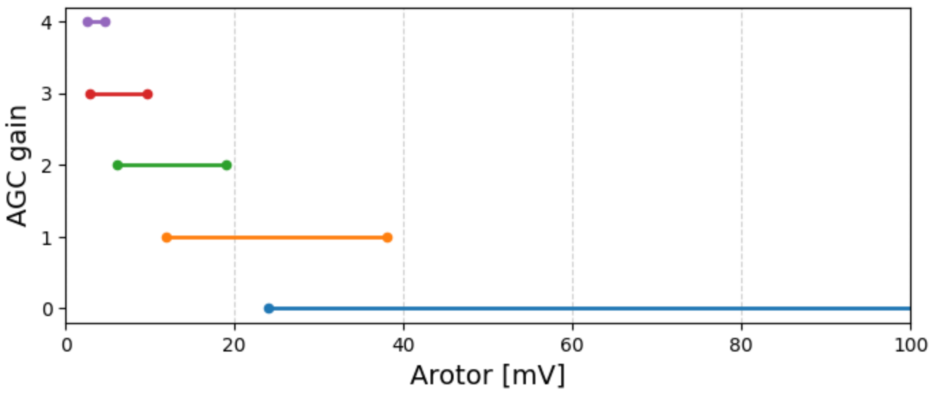


Figure 6: AGC gain settings as a function of A_{Rotor}

7.5 Digital Signal Processing (DSP)

The ADC permanently provides sequential samples to the DSP, including samples of the six INx input phase differences, LCO amplitude samples and functional safety test measures.

The DSP features two parallel tracks, one for channel A and one for channel B, each comprising a DC offset compensation, interpolation (to align all three phases to a common sampling point), conversion from 3-phase to I/Q domain, a tracking phase-locked loop and a linearization option. The output angles are compensated regarding processing delay utilizing estimated speed and acceleration, resulting in the two angles φ_{DLCA} and φ_{DLCB}.

The DSP features a difference angle, a mean angle, and a Vernier angle calculation unit which can work on any pair of the φ_{DLCA}, φ_{DLCB} angles.

7.5.1 Digital offset compensation methods

In Section 7.4.1 the composition of the INx signals is given. The signals $A_{Asym0A,B}$, $A_{Asym1A,B}$ and $A_{Asym2A,B}$ are DC offsets of the input signals of the A (INxA) and B (INxB) channels, respectively, being mainly caused by asymmetries of the PCB coil design (Rx and Tx coils), and caused by feeding lines from and to the sensor or metal objects close to the sensor. This asymmetry can be compensated in the MLX90514 by setting the fields DC01A [15:0], DC12A [15:0] and DC20A [15:0] for channel A, and DC01B [15:0], DC12B [15:0] and DC20B [15:0] for channel B. The compensation methods are fully automated in the PTC-04/PTC-05 programming tool. To ensure SIL 2 compliance and accuracy, it is mandatory to perform DC offset compensation.

The offset compensation is subject to thermal drifts whose magnitude is dependent on the LCO frequency and the ratio between the amount of compensated A_{Asym} and the useful signal strength A_{Rotor}. The thermal drift dependence on these two parameters is illustrated in Figure 7 assuming that the offset compensation is performed at 35 °C.

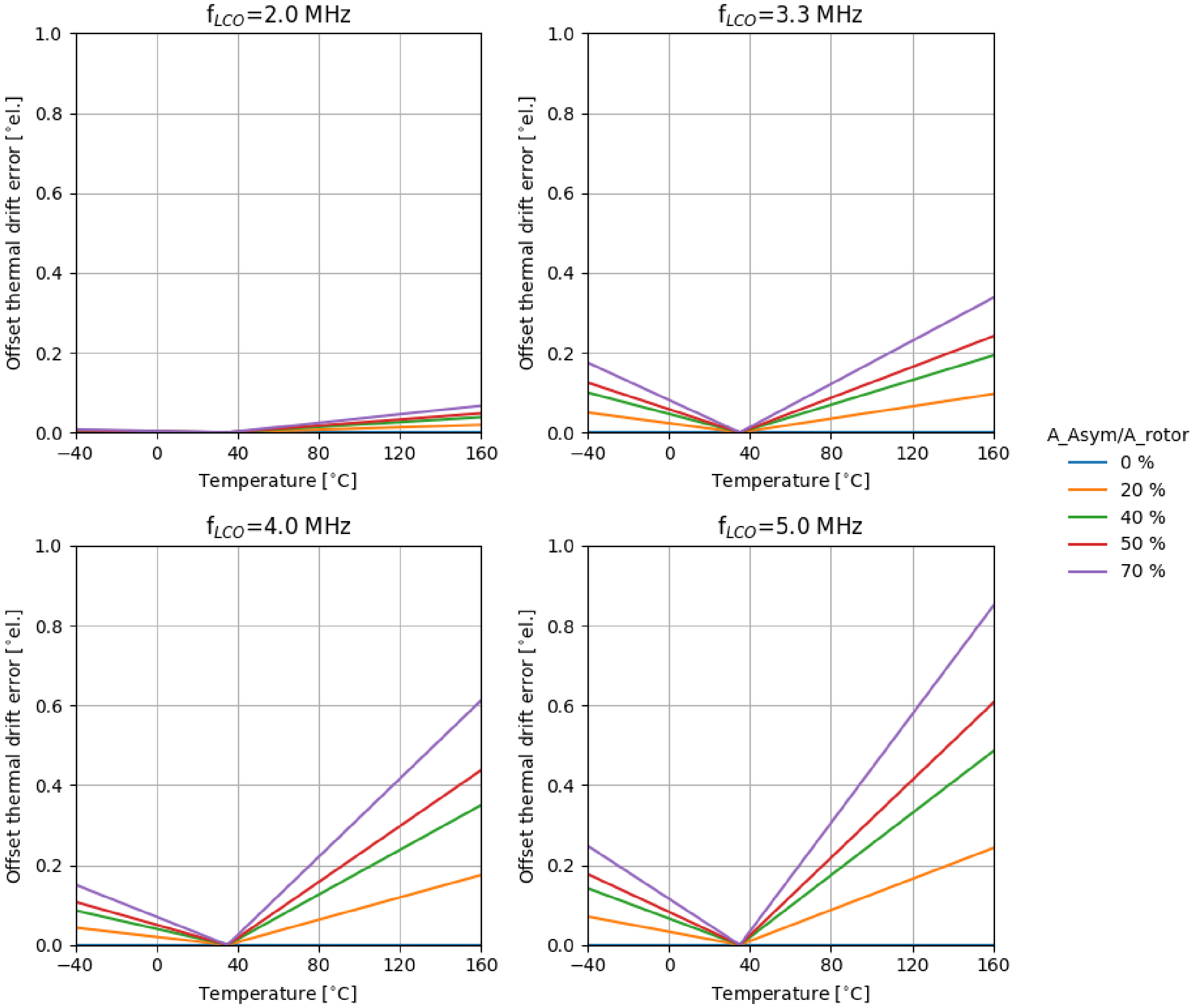


Figure 7: Offset thermal drift error

7.5.2 Phase tracking loop

The phase tracking loop calculates the angle, speed and acceleration of the input signals envelope per channel A and B. The phase tracking loop is characterized by a finite bandwidth that limits the maximum acceleration allowed for the input signals. The band-width (see of the tracking loop Figure 8) is determined by the loop filter coefficient (LFC), controllable via fields DSP_LFC_LO [2:0] and DSP_LFC_HI [2:0] , refer to Section 7.4.1.

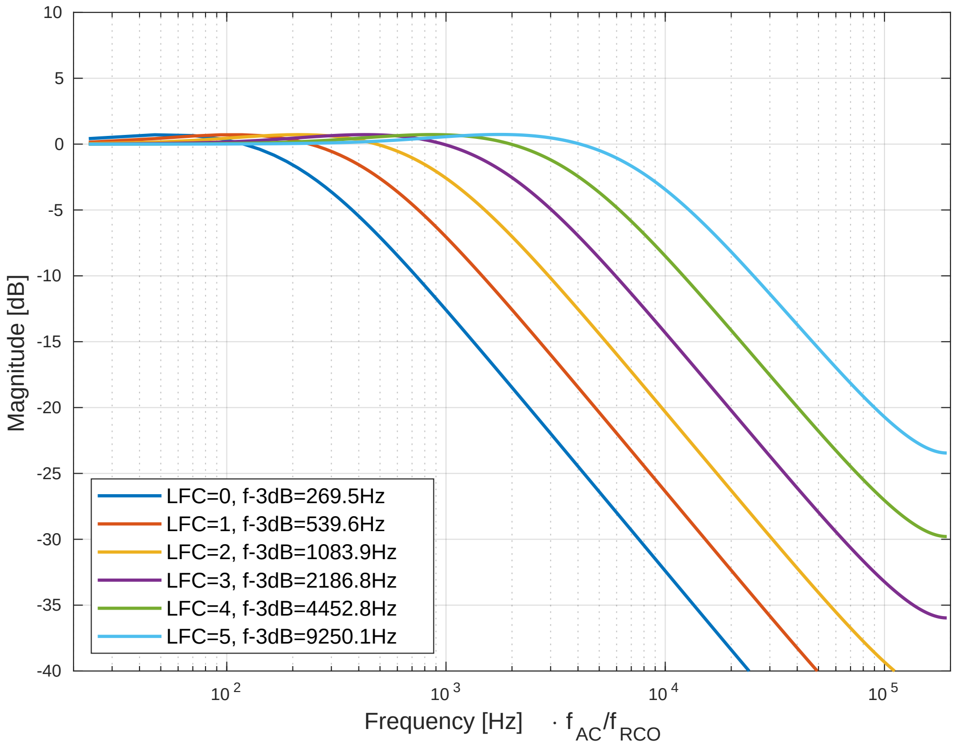


Figure 8: Phase tracking loop frequency response

The 16-bit 2's-complement angle estimates including linearization (refer to 7.5.3) reflect the electrical angle per channel as:

$$\varphi_{A/B}[^\circ el] = LIN\_PHASE_{A/B}/2^{16} \cdot 360^\circ el$$

The 17-bit 2's-complement speed estimates (range [-(2^{16}),2^{16}-1]) reflect the electrical rotational speed as:

$$v_{elA/B}[e\text{-}rpm] = \frac{SPEED\_HI_{A/B} \cdot 2^{16} + SPEED\_LO_{A/B}}{2^{23}} \cdot \frac{f_{AC} \cdot 60}{26}$$

Table 14 depicts the expected range of the electrical speed estimate depending on the application clock and whether the 16-bit or 17-bit SPEED value is evaluated.

f_{AC} [MHz]	{SPEED_HI, SPEED_LO} max(|v_{el}|) [e-rpm]	SPEED_LO max(|v_{el}|) [e-rpm]
20	350000	175000
10	175000	87500
5	87500	43750

Table 14: Electrical speed depending on f_{AC} and width of SPEED value

The RCO frequency tolerance limits the absolute accuracy of the rotational SPEED estimate. A calibration is possible via the synchronous interfaces (SPI) reading a free running period counter value PCNT [15:0], which runs continuously in range [0, PCNT_PERIOD-1] with time resolution $1/f_{AC}$. The PCNT counter needs to be enabled with PCNT_EN set to 1.

7.5.3 16-Point linearization

The 16-point linearization allows to equalize angular non-linearity errors which can be caused by asymmetries in the sensor coil system layout. Being a sub-block of the phase tracking DSP, the equalization works speed independent. Both the A and B channels dispose of dedicated linearization functions.

The 16 equalization values LINA00 [7:0] to LINA15 [7:0] (2's-complement, range [-(2^7),2^7-1]) characterize the angular error curve at angular sample points $[0 \ldots 15]/16 \cdot 360$ [°el] which is applied to the channel A angle. The values LINB00 [7:0] to LINB15 [7:0] apply for channel B likewise. All intermediate values are linearly interpolated, see Figure 9. After equalization, the residual error curve is the difference between the input error curve and the interpolated equalization curve. The characterization of the equalization coefficients LINAxy and LINBxy should be performed in quasi-static or low-speed application mode. With increasing rotational speed, the 16-point linearization automatically adapts to the low pass band limitation of the error curve.

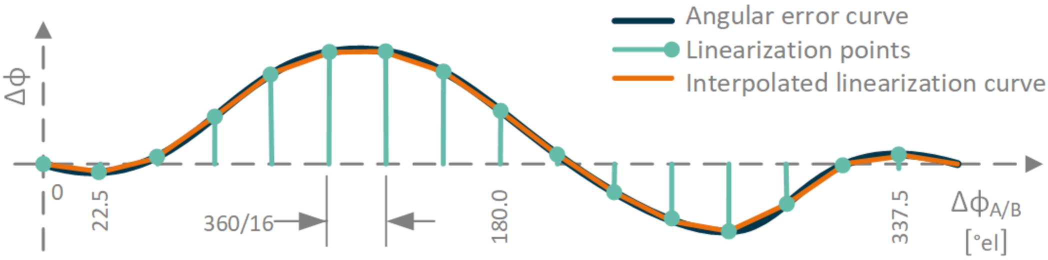


Figure 9: Angular error curve compensation

Depending on LINA_GAIN [2:0] and LINB_GAIN [2:0], the gain of the equalization curve can be adjusted for the A and B channels, respectively. If LIN[A,B]_GAIN is set to 0, no equalization is applied. For LIN[A,B]_GAIN = [1 ... 7] the error curve is adjusted per sample point as:

$$\Delta\varphi = signed\,(LIN[A,B]xy) \cdot 2^{LIN[A,B]\_GAIN-17} \cdot 360\,[^{\circ}el]$$

The signed 8-bit equalization values LIN[A,B]00 to LIN[A,B]15 have a range of [-127:127] each. Table 15 indicates the equalization range versus resolution per sample point.

LIN[A,B]_GAIN [2:0]	Resolution [deg]	Range (±) [deg]
0	0	0
1	0.0055	0.70
2	0.011	1.40
3	0.022	2.79
4	0.044	5.58
5	0.088	11.16

LIN[A,B]_GAIN [2:0]	Resolution [deg]	Range (±) [deg]
6	0.176	22.32
7	0.352	44.65

Table 15: Linearization range

The calculated angle after linearization and before delay compensation and zero position adjustment can be monitored via the register LIN_PHASE_A [15:0] and LIN_PHASE_B [15:0] (refer to Section 11.3).

The linearization is part of the phase tracking loop (refer to Section 7.5.2) making the angular equalization independent from rotational speed. During calibration of the equalization values it is advised to perform it at low rotational speed or configure the phase tracking loop filter to high bandwidth, (see Figure 8).

7.5.4 Delay compensation and zero position adjustment

The speed signal provided by the phase tracking loop (refer to Section 7.5.2) is used to compensate for phase errors due to the system latency, while the acceleration signal is used to compensate for phase errors during acceleration due to the latency of the speed calculation. The user furthermore disposes of the programmable field DELAY_ANA to compensate for additional delays associated to e.g. filter networks in between the IC and the ECU, in steps of $3.25/f_{RCO}$.

As a final complement, the mechanical position of the target resulting in zero output value for channels A and B can be adjusted by setting the fields PHASE_OFS_A[15:0] and PHASE_OFS_B[15:0], respectively. The values of these fields are systematically added to the position values calculated by the phase tracking loops.

The two calculated angles after delay compensation and zero position adjustment can be monitored via the register SC_FC1 [15:0] and SC_FC2 [15:0] (refer to Section 7.5.6), hereafter referred to as φ_{DLCA} and φ_{DLCB}.

7.5.5 Vernier angle calculation

The MLX90514 allows performing a Vernier angle calculation in between a primary angle PA and a secondary angle SA selected by the VER_CFG [2:0] field according to Table 16. The Vernier angle can be used for absolute position sensing.

VER_CFG	φ_{PA}	φ_{SA}
0	φ_{DLCA}	φ_{DLCB}
1	φ_{DLCB}	φ_{DLCA}

Table 16: Vernier inputs selection

Here φ_A, φ_B and φ_C denote the delay compensated 16-bit electrical angle values from sensor channel A and B respectively. Note that PA and SA need to have the same rotation direction for correct Vernier calculation.

The Vernier angle VA is calculated from PA and SA according to the following formula:

$$VA = mod\left(\frac{PA + 2^{16} \cdot mod\left(VM \cdot round\left(\frac{VDS \cdot PA - VDP \cdot SA}{2^{16}}\right), VDP\right)}{VDP}, 2^{16}\right)$$

Where VDP is the Vernier divider primary defined by the field VER_VDP [5:0], VDS is the Vernier divider secondary defined by the field VER_VDS [5:0] and VM is the Vernier multiplier defined by the field VER_VM [5:0]. VDP corresponds to the number of electrical periods of the PA angle over a Vernier angle range, while VDS corresponds to the number of electrical periods of the SA angle over a Vernier angle range.

For a correct VA result VM needs to be configured to satisfy the following conditions:

$$mod\left((VDP - VDS) \cdot VM, VDP\right) = 1$$
$$VM < max(VDP, VDS)$$

For high resolution it is recommended to choose $VDP > VDS$.

An illustrative case of Vernier calculation is depicted in Figure 10, where the primary angle PA has 5 periods and the secondary angle SA has 3 periods per mechanical rotation. The Vernier angle VA represents 1 mechanical rotation.

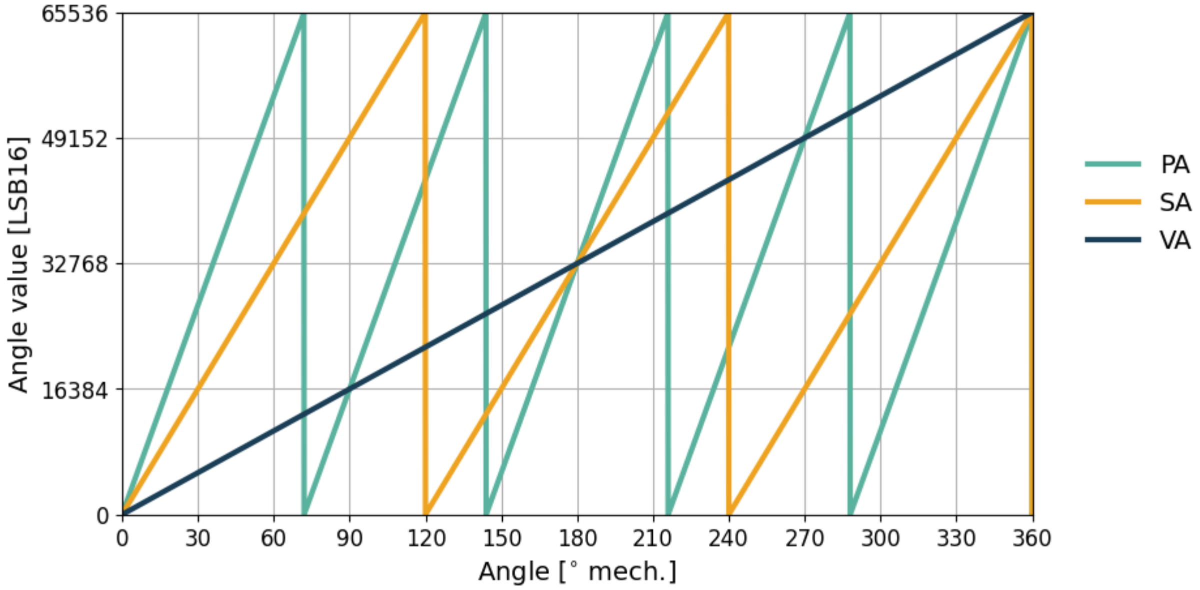


Figure 10: Example of Vernier calculation for VDP=5, VDS=3 and VM=3

The zero point of Vernier angle value depend on the zero point of the primary angle as:

$$VA_0 = \frac{PA_0}{VDP} \cdot \frac{2^{16}}{360}$$

For a robust calculation of the Vernier angle the primary and secondary angle should have the same mechanical zero position. Any offset between PA and SA can be determined by the Vernier reserve diagnostic DIAG_VRES, refer to 10.5.5. The 16-bit 2's-complement Vernier reserve value is computed as:

$$VRES = mod\left(mod\left(PA \cdot VDS + 2^{15}, 2^{16}\right) - mod\left(SA \cdot VDP, 2^{16}\right), 2^{16}\right) - 2^{15}$$

VRES near to +/-2^{15} will lead to selection of a wrong Vernier-section and corresponds to offsets of $\Delta SA\,[°\text{el}] = \pm 180\,°\text{el}/VDP$ or $\Delta PA\,[°\text{el}] = \pm 180\,°\text{el}/VDS$.

The VA accuracy depends only on PA as long as distortions or offsets on SA do no exceed the range $\pm 180\,°\text{el}/VDP$.

7.5.6 Fast Channel mapping

The MLX90514 DSP supports two synchronous fast channel signal paths towards the output interfaces with independent signal conditioning according to the selected output mode. Any sensor path angle value or the computed result for Vernier angle can be mapped onto these fast channels.

7.5.6.1 Fast Channel 1 (FC1)

The Fast Channel 1 (FC1) content can be selected by field FC1_CFG [2:0] per Table 17. The Fast Channel 1 can be transferred via all interfaces, see Section 8.

FC1_CFG [2:0]	FC1 [15:0]
0	φ_{DLCA}, refer to Section 7.5.4
1	φ_{DLCB}, refer to Section 7.5.4
2,3,4	Reserved
else	VA, refer to Section 7.5.5

Table 17: Fast Channnel 1 configuration

7.5.6.2 Fast Channel 2 (FC2) with time-multiplexing

The Fast Channel 2 (FC2) additionally allows to change its content over time based on the 2 LSB of the internal rolling counter (RC) of the SPI interface. The Fast Channel 2 is captured synchronously with FC1.

RC [1:0]	FC2 [15:0]
0	FC2_0
1	FC2_1
2	FC2_2
3	FC2_3

Table 18: Fast Channel 2 time-multiplexing

The FC2 content can be selected by fields FC2_CFG* [2:0] per Table 19. If any of the fields FC2_CFG_RC* is set to zero, the configuration of FC2 for RC time slot 0 (FC2_0) is transmitted. By default, the time-multiplexing is disabled (FC2_CFG_RC1 = FC2_CFG_RC2 = FC2_CFG_RC3 = 0).

FC2_CFG [2:0] FC2_CFG_RC1, FC2_CFG_RC2, FC2_CFG_RC3	FC2_0 [15:0]	FC2_1 [15:0], FC2_2 [15:0], FC2_3 [15:0]
0	φ_{DLCA}, refer to Section 7.5.4	FC2_0 [15:0]
1	φ_{DLCB} , refer to Section 7.5.4	
2,3,4	Reserved	
5	VA, refer to Section 7.5.5	
6,7	0	

Table 19: Fast Channel 2 configuration

7.5.7 Signal Conditioning

The MLX90514 is equipped with two signal conditioning units which allow adapting the DSP angles of interest to the output protocol dependent signaling ranges. The two signal conditioning units operate on the selected fast channel values FC1, see Section 7.5.6.1, and FC2, see Section 7.5.6.2. The FC1 signal conditioning is configurable by the 16-bit fields SC1_X1, SC1_X2, SC1_Y1 and SC1_Y2, while the FC2 signal conditioning makes use of SC2_X1, SC2_X2, SC2_Y1 and SC2_Y2 respectively. Figure 11 illustrates the main steps.

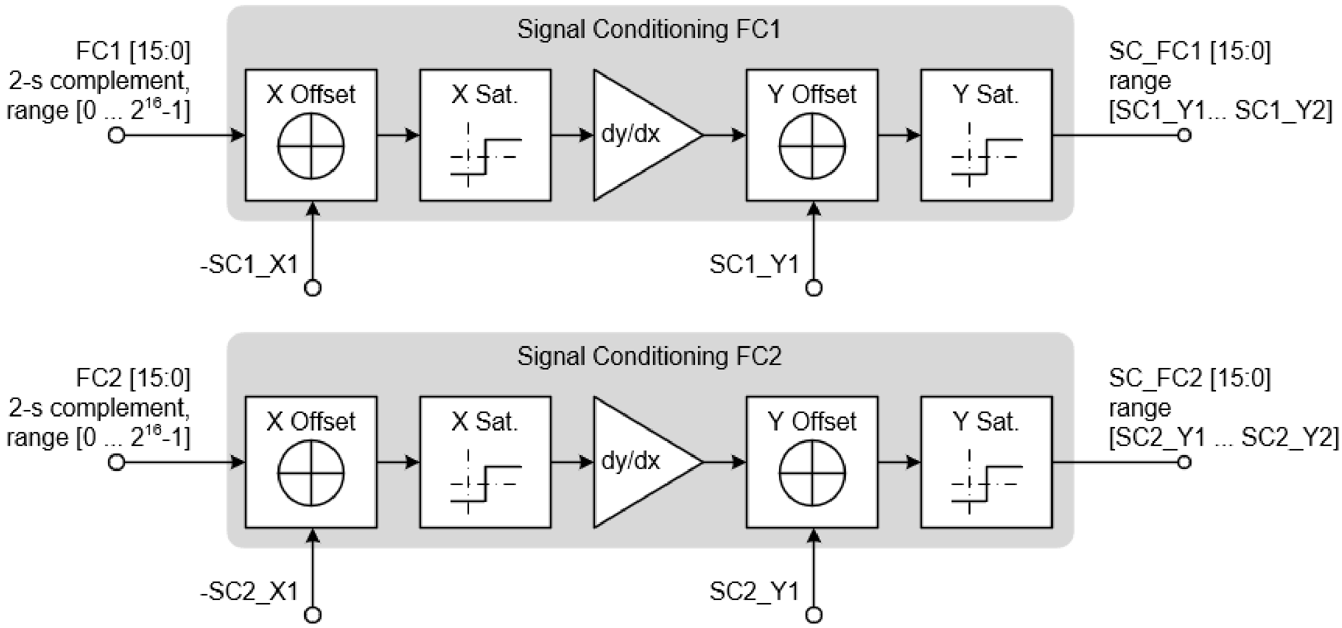


Figure 11: Signal conditioning procedure

The input stage, defined by 2's-complement values SC[1,2]_X1 [15:0], SC[1,2]_X2 [15:0], restricts the angle of interest and saturates all measured angles exceeding the range [SC[1,2]_X1 .. SC[1,2]_X2]. Note that there is no limitation on the value of SC[1,2]_X1 vs SC[1,2]_X2. Input range selection overlapping with the zero-point is possible, e.g. [SC[1,2]_X1 = -8192 (signed) = 57344 (unsigned) , SC[1,2]_X2 = 8191 (signed/unsigned)] selects the electrical angle range [-45 ° .. <45 °].

This stage can be bypassed by setting [SC[1,2]_X1, SC[1,2]_X2] = [0,0] or [0, 2^16-1]. The gain stage scales the signal with the ratio of output range width to the input range width.

The output stage, defined by 2's-complement values SC[1,2]_Y1 [15:0], SC[1,2]_Y2 [15:0], adds the offset SC[1,2]_Y1 and saturates values exceeding the output range [min(SC[1,2]_Y1, SC[1,2]_Y2) ... max(SC[1,2]_Y1, SC[1,2]_Y2)]. It is recommended to understand SC[1,2]_Y1 and SC[1,2]_Y2 here as unsigned values in range [0 .. 2^16-1] and that in the linear transformation SC[1,2]_Y1 refers to SC[1,2]_X1, while SC[1,2]_Y2 refers to SC[1,2]_X2 respectively. This means that if SC[1,2]_X1 < SC[1,2]_X2 but SC[1,2]_Y1 > SC[1,2]_Y2 the transfer characteristic is inverted.

This stage can be bypassed by setting [SC[1,2]_Y1, SC[1,2]_Y2] = [0,0] or [0, 2^16-1].

Within the saturated region, the occurrence of the transition between the SC[1,2]_Y1 and SC[1,2]_Y2 defined outputs can be controlled via the SC1_HL [7:0] and SC2_HL [7:0] parameters. SC[1,2]_HL [7:0] defines the offset of the transition point from the center point (SC[1,2]_X1+SC[1,2]_X2)/2, in units of $360\,°/2^8$.

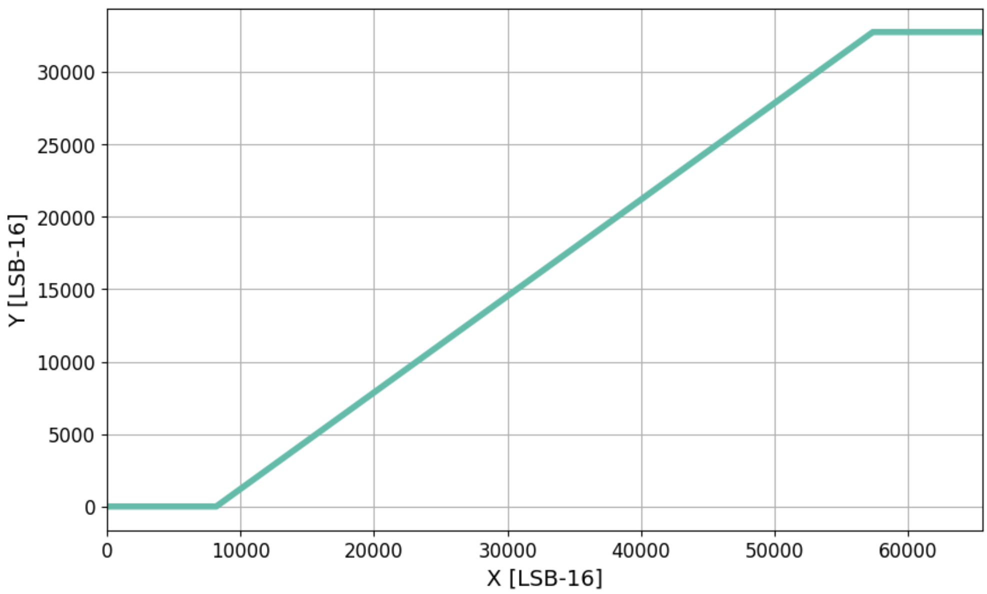


Figure 12: SC transfer curve for FC1 with SC1_X1=8192; SC1_X2=57343; SC1_Y1=0; SC1_Y2=2^{16}-1, SC1_HL=0

Figure 12 depicts a configuration intended for 15-bit SSI output (valid signal range: [0 .. 2^{16}-1]) and an input range restriction from 45 ° to -45 ° (span 270 °).

The signal condition transformation influences the signal resolution as follows:

Parameter	Symbol	Resolution	Unit
Resolution of electrical angle	R_{angle_el}	$360/2^{16}$	deg
Resolution of angle after signal conditioning	R_{angle_SC}	$\frac{360}{2^{16}} \cdot \frac{\max(1, \lvert \text{unwrap}(\text{SC[1,2]\_X2} - \text{SC[1,2]\_X1}) \rvert)}{\lvert \text{SC[1,2]\_Y2} - \text{SC[1,2]\_Y1} \rvert}$	deg

Table 20: Signal conditioning resolution

The following settings for SC[1,2]_Y1 [15:0], SC[1,2]_Y2 [15:0] are recommended for different output modes to comply to valid signal ranges.

MODE	SC1_Y1 [15:0]	SC1_Y2 [15:0]	SC2_Y1 [15:0]	SC2_Y2 [15:0]	Comment
SPI, FR	0	0	0	0	16-bit for FC1 and FC2
SSI, FR	0	0	0	0	16-bit for FC1 and FC2
SSI, conventional	0	2^{15}-1	0	0	15-bit for FC1 (FC2 not transmitted)

Table 21: Signal condition settings for different output modes

The signal values after signal conditioning can be monitored via the register SC_FC1 [15:0] and SC_FC2 [15:0], refer to Section 11.3.

7.5.7.1 Fault band mapping

For functional safety in case of detected errors leading to safe state SS3, the signal conditioning outputs on fast channel 1 the fault band value as defined by field SC1_YE [15:0].

If SC1_YE is configured with a value within the output range (min(SC1_Y1, SC1_Y2) to max(SC1_Y1, SC1_Y2)) or if in case of a missing output range (e.g. SC1_Y1 = SC1_Y2) a fault band reporting is impossible and the MLX90514 switches to the output safe state SS2 (Hi-Z), except for SPI. In SPI (FR), in this case, the data value is transmitted and the safe state information must be transmitted via the enabled frame start byte.

8 Output modes

This chapter describes the output interfaces of the MLX90514. The output mode can be selected with the field PROTOCOL [2:0].

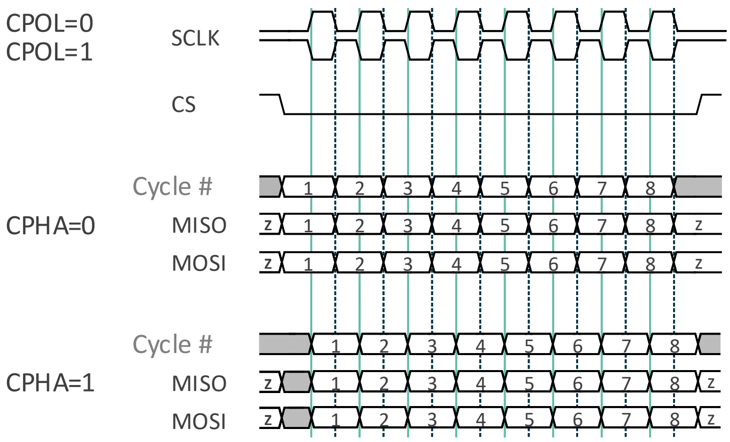
PROTOCOL [2:0]	Output Mode
2	SSI
4	SPI (bus mode)
else	reserved

Table 22: Output mode selection

8.1 Serial Peripheral Interface (SPI)

The MLX90514 features a full-duplex slave high-speed SPI for sensor data transfer and device programming. An SPI transmission can be started with the active-low pin CS and will override any other configured output interface. However, with PROTOCOL [2:0] = 4 the SPI mode operates exclusively.

All standard SPI timing modes are supported by field SPI_MODE [1:0].



SPI_MODE [1:0]	Clock polarity (CPOL)	Clock phase (CPHA)
0	0	0
1	0	1
2	1	0
3	1	1

Table 23: SPI timing mode

8.1.1 SPI transactions

The SPI supports memory and register read / write access and continuous readout with functional safety protections which can be synchronized over multiple slaves.

Transaction are started with a command byte from MOSI, see Table 24.

Command	Command code	Description
RD	6’b110011	Register Read, see Section 8.1.1.1
WR	6’b011110	Register Write, see Section 8.1.1.2
FR	6’b000000	Frame Read, see Section 8.1.1.3
SFR	6’b110100	Super Frame Read, see Section 8.1.1.4

Table 24: SPI commands

In case of receiving an invalid command byte the IC defaults to sensor data transfer (FR). If MISO does not carry data, it returns the previous MOSI byte denoted as MOSI(k-1).

The SPI protocol comprises the MSB-1st byte-wise basic transactions “Register Read” (RD), “Register Write” (WR) and “Frame Read” (FR), see Figure 13. Each line depicts an SPI byte transfer on MISO and MOSI respectively. Unused values from MOSI are not displayed. Greyed fields are optional.

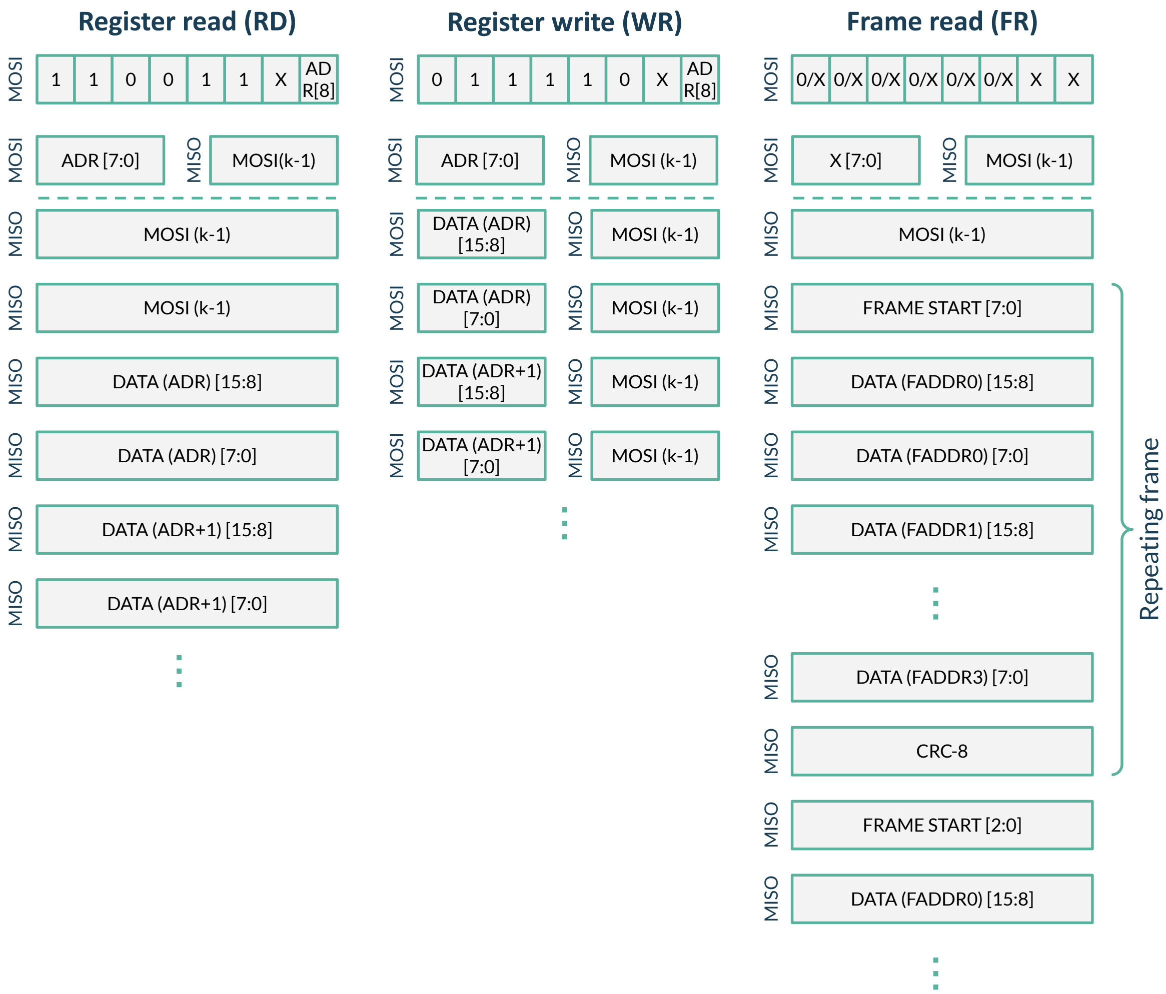


Figure 13: MLX90514 basic SPI transactions

8.1.1.1 Register Read (RD)

”Register Read” (RD) allows DMA read access to device registers or memory, starting from the 16-bit word aligned address {A8, ADR [7:0], 1'b0}, which covers the complete IC address range including EEPROM. With SPI_DMY [0] = 1 an additional delay byte can be introduced which allows adjusting the word alignment of the data transfer.

The RD command features auto-address-increment, which allows to read out a sequence of registers as long as CS remains in active state.

8.1.1.2 Register Write (WR)

”Register Write” (WR) allows DMA write access to device registers or memory, starting from the 16-bit word aligned address {A8, ADR [7:0], 1'b0}, which covers the complete IC address range including EEPROM.

While the 16-bit write data per address is transmitted in 2 bytes on MOSI, the previous transfer can be verified with MISO (k-1). Note that this data is the content of the SPI shift register, not the content of the target address.

The WR command features auto-address-increment, which allows to write a sequence of registers as long as CS remains in active state.

8.1.1.3 Frame Read (FR)

“Frame Read” (FR) allows a sequential and repeated read-out of up to 4 pre-configured register address values comprising a frame:

1. {1’b0, SPI_FADDR0 [7:0], 1’b0} : default pointing to register SC_FC1 [15:0]
2. {1’b0, SPI_FADDR1 [7:0], 1’b0} : default pointing to register SC_FC2 [15:0]
3. {1’b0, SPI_FADDR2 [7:0], 1’b0} : default pointing to 0x00 (not transmitted)
4. {1’b0, SPI_FADDR3 [7:0], 1’b0} : default pointing to 0x00 (not transmitted)

If SPI_FADDR0 [7:0] = 0, register SC_FC1 [15:0] is transferred (DSP Fast Channel 1). If SPI_FADDR1 or SPI_FADDR2 or SPI_FADDR2 are set to 0, the corresponding values are skipped.

A frame start-byte (FS) can be prepended to each frame when configured with SPI_FRFSEN = 1. The FS is composed of a 4-bit programmable frame start pattern SPI_FRFS [3:0] and a 4-bit rolling counter, which is incremented per frame:

FS [7:0] = { SPI_FRFS [3:0], RC [3:0] }

Each frame can be protected by a CRC-8 sequence when configured with SPI_FRCRCEN = 1. The frame check sequence of type CRC-8-CCITT includes all data value and the optional frame start byte with the generator polynomial:

$$x^8 + x^2 + x + 1$$

With SPI_DMY [1] = 1 an additional delay byte can be introduced before the first data frame which allows adjusting the word alignment of the data transfer.

SPI_FRINV [3:0] allows to binary invert the transferred data words of FADDR0 ... FADDR3 by setting the corresponding bit. This can be used as an alternative data protection method in conjunction with repetitive data transfer.

In FR mode the transmission of frames is continued as long as CS remains in active state.

Fast channel data (SC_FC1, SC_FC2) is captured from the DSP at the beginning of each frame before the DATA (FADRR0) [15:8] byte, see Figure 14.

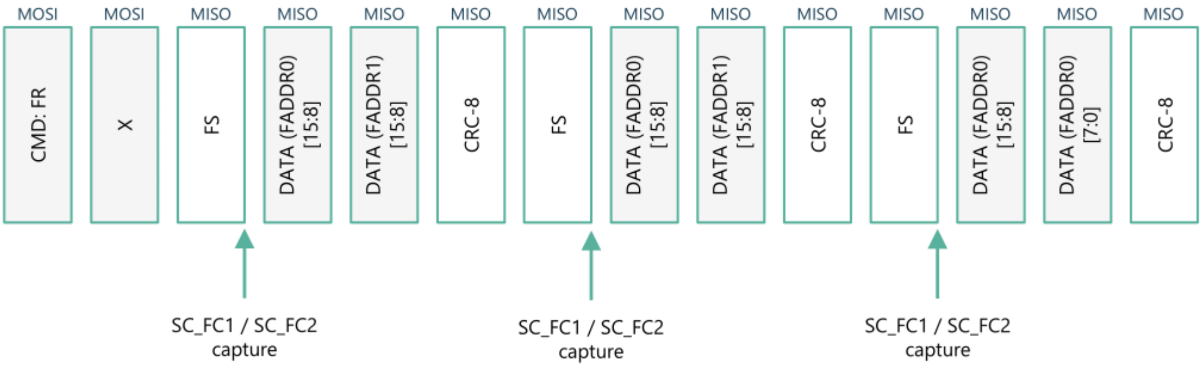


Figure 14: DSP Fast Channel data capture points for FR with 2-byte DATA + FS + CRC-8

The DSP capturing lead time can be controlled to (SPI_CPTLT [2:0] + 1) / f_{SCLK} before SCLK sampling edge of the DATA(FADDR0) [15] (MSB). Both fast channels are synchronously sampled. For f_{SCLK} > 2 MHz, SPI_CPTLT must be ≥ 1 to not violate the bus access duration SPI_t_{BUS}, refer to Section 8.1.2.

Other DMA registers are captured with a lead time of ($8/f_{SCLK} - 2/f_{AC}$) before the SCLK sampling edge of DATA(FADDRx) [15].

8.1.1.4 Super Frame Read (SFR)

The command code 6’b110100 initiates a Super Frame Read (SFR) transaction, which allows the synchronous Fast Channel data capture and sequential TDMA transmission with multiple SPI slaves sharing the same MISO bus. Figure 15 shows an example of a configuration with 2 devices, with a FR configuration with only FS + DATA (FADDR0) + CRC-8, e.g. to transfer the DSP fast channel SC_FC1.

A super frame is configured by its frame length in bytes SPI_SFRL [7:0], which defines the period after which each slave repeats capturing data and transmitting this data in a single FR frame. SPI_SFRL should be configured equal for all participating SPI SFR slaves and needs to be greater than the sum of all FR frames lengths from these slaves.

SPI_SFRDLY [7:0] allows to configure the individual transmission delay in bytes per SPI SFR slave. After start of the super frame each device will keep signal MISO in Hi-Z for SPI_SFRDLY · 8 SCLK cycles before starting a transmission of the individual FR configuration.

As shown in Figure 15, the SPI_SFR_SCPT bit gives 2 options for the capturing of the Fast Channel DSP data into the SFR frames.

SPI_SFR_SCPT	DSP Fast Channel capture timing
0 (default)	Each slave captures at (SPI_CPTLT [2:0] + 1) / f_{SCLK} before SCLK sampling edge of the DATA(FADDR0) [15] of their FR response
1	All slaves capture at (SPI_CPTLT [2:0] + 1) / f_{SCLK} before SCLK sampling edge of the DATA(FADDR0) [15] as for SPI_SFRDLY = 0

Table 25: SPI super frame capture timing

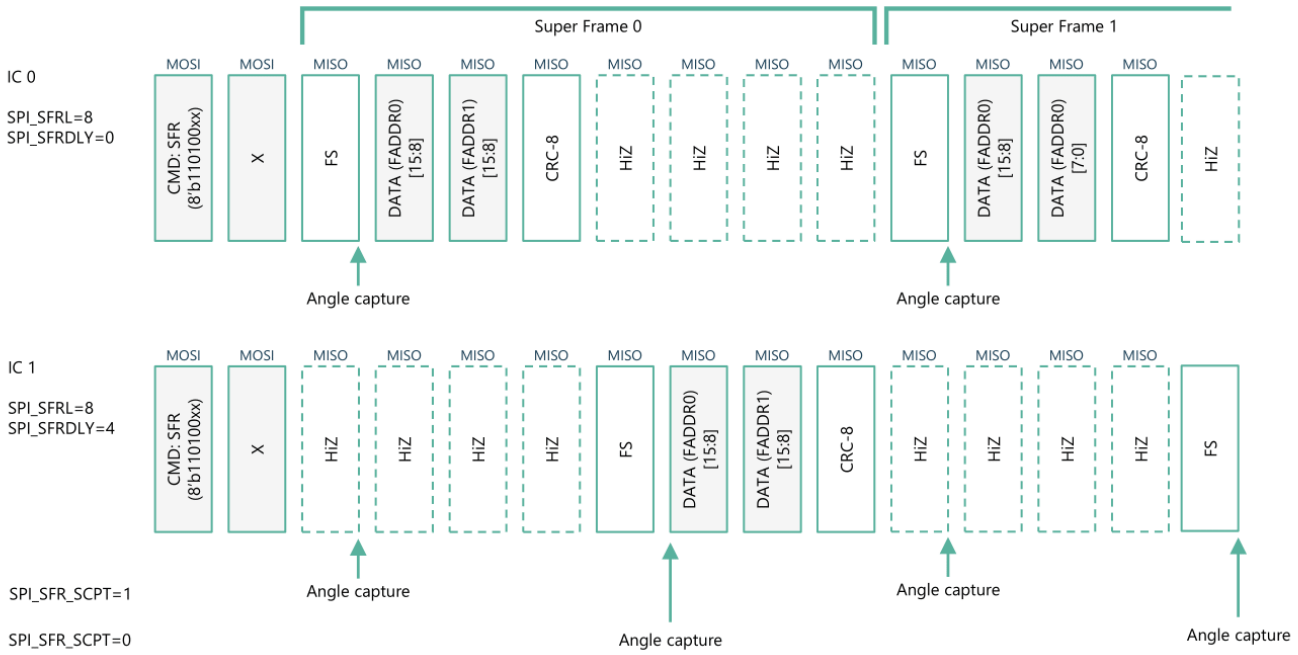


Figure 15: Super Frame configuration with 2 SPI slave devices on shared MISO bus

8.1.2 SPI timing characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SPI clock frequency	f_{SCLK}	0.04		10	MHz	EMC filter off, $f_{AC} > f_{SCLK}/2$
SPI CS active until SCLK active edge delay	SPI_t_{CS0}	0.5			$1/f_{SCLK}$	PROTOCOL = SPI, SPI_DBNC = 0, SPI_DBNC_CS = 0
		250			ns	PROTOCOL ≠ SPI, SPI_DBNC = 0, SPI_DBNC_CS = 0

Parameter	Symbol	Min	Typ	Max	Unit	Condition
SPI inactive delay after SCLK active edge	SPI_t_{CS1}	4			$1/f_{AC}$	SPI WR
		1			$1/f_{SCLK}$	SPI RD, FR, SFR
SPI idle time	SPI_t_{IDLE}	1			$1/f_{SCLK}$	
SPI MISO enable delay after CMD byte	SPI_t_{OE}			200	ns	SPI_DBNC = 0, CMD OK
SPI MISO disable delay after CS inactive	SPI_t_{OD}			200	ns	SPI_DBNC = 0
SPI MISO data delay	SPI_t_{SDO}			40	ns	$C_L \leq 20$ pF
SPI bus access duration	SPI_t_{BUS}			4	$1/f_{AC}$	

Table 26: SPI timing parameters

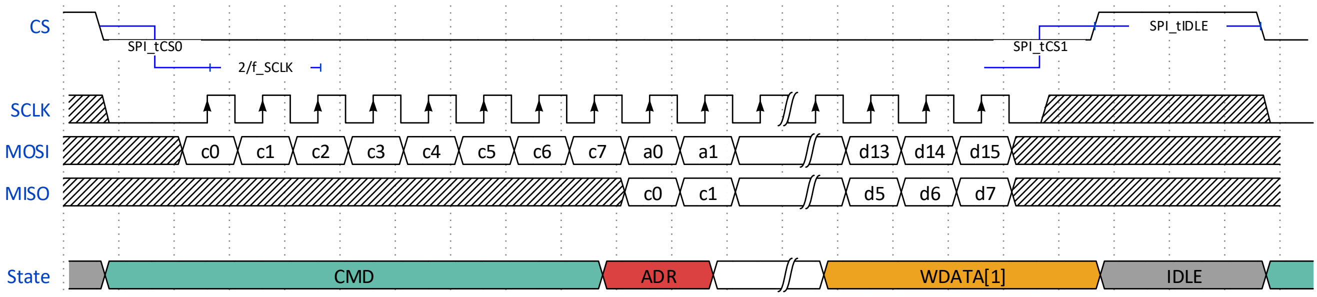


Figure 16: SPI timing example for SPI_WR

The SPI offers digital debouncing for the signals MOSI, SCLK and CS, which can be controlled with fields SPI_DBNC [3:0] and SPI_DBNC_CS [3:0] respectively. This debouncing creates following delays:

- τ_{SCLK} (SPI_DBNC) = τ_{MOSI} (SPI_DBNC) = SPI_DBNC / f_{RCO}
- τ_{CS} (SPI_DBNC_CS) = 2·SPI_DBNC / f_{RCO}

These delays lead to a limitation of the SPI clock frequency: f_{SCLK} < 0.4 / (SPI_t_{SDO} + (SPI_DBNC+1)/f_{RCO}). Also, SPI_t_{CS0} is influenced:

- if SPI_DBNC_CS > 0: SPI_t_{CS0} > (2·SPI_DBNC_CS+1) / f_{RCO}
- if SPI_DBNC > 0: SPI_t_{CS0} > (SPI_DBNC+1) / f_{RCO}

8.2 Synchronous Serial Interface (SSI)

The MLX90514 features a Synchronous Serial Interface (SSI) for embedded applications, supporting simple data output as well as a safety-enhanced protocol aligned to SPI FR, refer to Frame Read (FR) Section 8.1.1.3. SSI is activated with PROTOCOL=2.

The SSI physical layer timing is depicted by Figure 17. SSI drives the SSI output signal on pin MISO clocked by pin SCLK. The supported SCLK frequencies of the SSI are the same as in SPI mode (f_{SCLK}), see Table 26. The communication follows the following sequence:

- In idle state, SCLK is on a H level and the sensor SSI output is on a H level, which enables detection of an open connection.
- After n-SCLK pulses (rising edges), the data is completely transmitted.
- With the next SCLK pulse (rising edge n+1), the SSI output goes to a L level which enables detection of a shorted connection.
- T_m: Transfer timeout (monoflop time). It is the minimum time required by the slave (the MLX90514 IC) to realize that the data transmission is complete. After T_m, the SSI goes to idle (H) and the slave starts updating its data in the shift register. Field SSI_TM [7:0] allows to set $T_m = (SSI\_TM + 1) \cdot 8/f_{AC}$.
- T_p: Pause time between 2 consecutive clock sequences. $T_p > T_m + 0.5\,\mu s$ should be respected

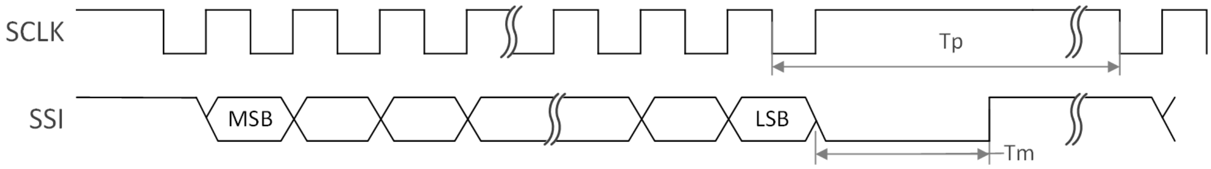


Figure 17: SSI general timing with FC1 data capture points

8.2.1 SSI frame format

8.2.1.1 SSI Frame Read (FR) mode

With SSI_FR = 1 the SSI returns a frame format compliant to SPI FR starting from the optional byte controlled by SPI_DMY [1], refer to Section 8.1.1.3. This includes the capturing of fast channel data according to SPI_CPTLT [2:0], see Figure 14. The SSI transfer timeout T_m in this case acts like CS in SPI.

Figure 18 provides an example of SSI communication in FR mode for Vernier output with following configuration: SSI_FR = 1, SPI_DMY = 0 (no dummy byte), SPI_FRFSEN = 1 and SPI_FRFS = 5 (frame start byte with pattern 4'b0101), SPI_FADDR0 = 0 (FC1), SPI_FADDR1 = SPI_FADDR2 = SPI_FADDR3 = 0 (not transmitted), SPI_FRCRCEN = 1 (CRC enabled), and FC1 set up to transmit the Vernier angle. The top diagram shows the behavior in case of pause between two SCLK sequences. The bottom diagram shows the behavior in case of uninterrupted SCLK sequence

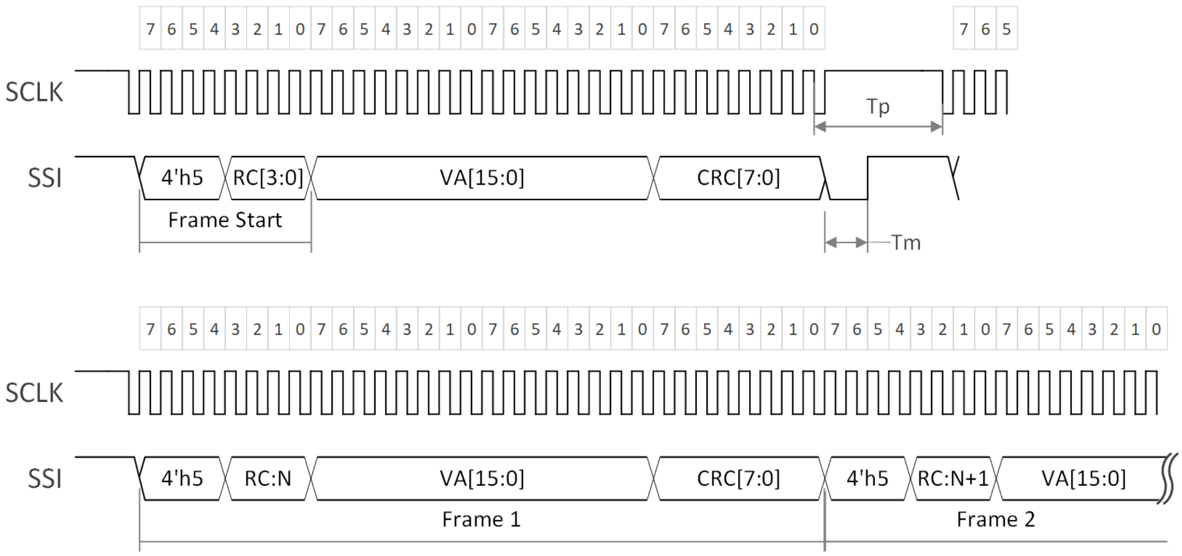


Figure 18: SSI FR application example for Vernier output protected by CRC and rolling counter

Note, that to achieve logic zero during T_m the MSB of the transmitted first payload byte must be zero.

8.2.1.2 SSI conventional mode

If bit SSI_FR = 0 the SSI operates in conventional mode transmitting a sequence of 16-bit FC1 values, refer to Section 7.5.6.1. The fast channel data capture time can be controlled by SSI_CPT as depicted by Figure 19.

SSI_CPT	DSP fast channel capture timing
0 (default)	falling edge on SCLK after startup or pause time T_p
1	T_m after rising edge on SCLK of pause time T_p

Table 27: SSI data capture time

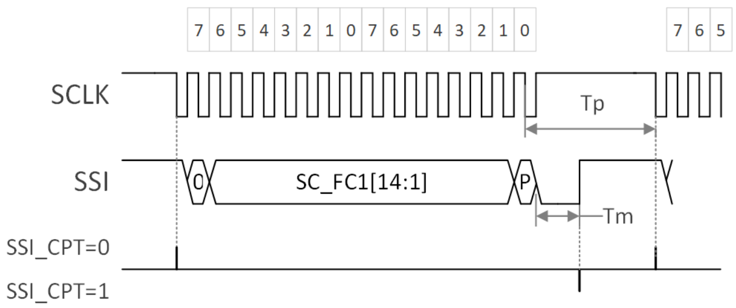


Figure 19: SSI frame format with parity

To ensure a correct generation of L at SSI output during T_m, the FC1 needs to be configured such that MSB of after signal condition is 0, e.g. with SC1_Y2 = 0x7fff instead of 0x0000 (default) .

The MLX90514 allows to transmit a parity bit with a programmable position (SSI_PARPOS [3:0]) w.r.t the SSI data value see Table 28. This enables the adjustment of the SSI word length by appending the pause time immediately after the parity bit position.

SSI_PARPOS	SCLK cycles per frame until T_m	Data resolution SSI=L on T_m	Data resolution SSI=H/L on T_m
0 (default)	16	14 bit	15 bit
1	15	13 bit	14 bit
2 ...8	16 - SSI_PARPOS	14 - SSI_PARPOS bit	15-SSI_PARPOS bit
>8: no parity bit	16	15 bit	16 bit

Table 28: SSI frame configurations with parity

Re-transmission is correctly supported for configurations with 16 SCLK cycles per frame.

With a modified SSI protocol and no parity bit the full 16-bit data can be transferred if SSI_PARPOS > 8 and SC1_Y2=0x0000 (default).

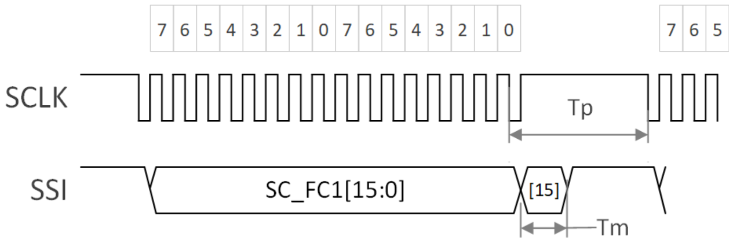


Figure 20: SSI frame format without parity and 16-bit data

9 Identification items

To ensure traceability and unique identification of the individual parts, the EEPROM stores read-only identifiers for the wafer fab (D_FAB_ID [3:0]), for the wafer lot (D_LOT_ID_HI [5:0], D_LOT_ID_LO [10:0]), for the wafer number within the lot (D_WFR_ID [4:0]), and the X and Y coordinates of the chip within the wafer(D_X_POS_ID [7:0] and D_Y_POS_ID [7:0], respectively), see Section 11.

Additionally, the user disposes of six fields that are freely programmable to arbitrary values: USER_ID0 [7:0] ... USER_ID5 [7:0].

10 Functional Safety

According to IEC61508, the MLX90514 achieves SIL 2. The technical safety concept is described in the ”Safety Manual IEC61508 : MLX90514 - Robotics and Industrial”.

In case of random internal failure detection, the MLX90514 transitions to one of its safe states: it either set its output pin MISO in a high impedance state (Hi-Z) or indicates safe state trough the output-protocol specific fault reporting, as long as the failure is detected.

10.1 Safety Manual

The Safety Manual, available upon request, contains the necessary information to integrate the MLX90514 component in a safety related item, as Safety Element Out-of-Context (SEooC).

In particular, it includes:

1) The description of the Product Development lifecycle tailored for the Safety Element
2) The overall technical safety requirements
3) An extract of the Technical Safety concept
4) The description of Assumptions-of-Use (AoU) of the element with respect to its intended use, including:
    - assumptions on environmental and functional condition
    - assumptions on external safety mechanisms
    - assumptions on end of line calibration
5) The description of safety analysis results and device-level hardware metrics that are useful for the system integrator
6) A summary of the functional safety assessment and its conclusions

10.2 Safety specification

The overall technical safety requirements of the MLX90514 are summarized in Table 29. Please refer to the Safety Manual for more details and boundary conditions. FHTI is given for $f_{AC} = 20$ MHz.

Description	Angle error	SIL	FHTI
The measured electrical angle for channel A and B shall not exceed an error θ_{FS} without safe state indication.	$\theta_{FS} = \pm 3$ °el	SIL 2	4 ms
The Vernier angle shall not exceed an error θ_{ver_FS} without safe state indication.	$\theta_{ver\_FS}[°\text{mech}] = \frac{\theta_{FS}}{VDP}$	SIL 2	4 ms

Table 29: Functional safety specification

10.3 Safe States

In all fail-safe states, the sensor application function and the LCO remains active until the fault condition forces an internal halt.

10.3.1 Safe State 2

Safe State 2 (SS2) reports critical faults, which may impact controlled reporting through the output interface. State SS2 has priority over SS3.

In SS2, pin MISO is switched to tri-state (high impedance Hi-Z) for all application output protocols. In conjunction with a pull-up resistor R_{PU} to VS placed at the corresponding ECU inputs, the IC indicates failure-band-high. In conjunction with a pull-down resistor R_{PD} to GND placed at the corresponding ECU inputs, the IC indicates failure-band-low.

Note that in SS2 the SPI programming transactions Register Read and Register Write are still supported as far as possible, while Frame Read and Super Frame Read commands return Hi-Z on pin MISO.

10.3.2 Safe State 3

Safe state 3 (SS3) is the default reporting mode for all faults which do not affect the operation of the output interface. In safe state SS3 the output interface remains active and reports the fault as part of the protocol as follows:

Interface	SS3 reporting
SPI (FR)	• The frame start field is binary inverted.
SSI	• SSI_FR=1 : The frame start field is binary inverted. • SSI_FR=0 : pin MISO is switched tri-state, see Section 10.3.1

Table 30: SS3 reporting overview per interface

Note that transitions to SS3 during SPI frame transmissions can cause CRC-errors for that frame.

10.4 Safety mechanism and monitors

Table 31 depicts the list of built in diagnostics or safety mechanisms. For more details refer to the Safety Manual.

Safety mechanism	Description	Safe state
AFE / Sensor diagnostics		
DIAG_LC_A	LCO amplitude difference monitor	SS3
DIAG_LC_P	LCO period monitor	SS3
DIAG_LC_OC	LCO overcurrent monitor	SS3
DIAG_SSL	Sensor short / loss monitor	SS3
DIAG_TRIA	Tri-Amp monitor	SS3

Safety mechanism	Description	Safe state
DIAG_FE	Frontend monitor	SS3
DIAG_AGC	AGC monitor	SS3
DIAG_ADC_LIN	ADC linearity selftest	SS3
Digital-IC Diagnostics		
DIAG_NVM_ECC	EEPROM double-bit error	SS2
DIAG_NVM_SR	EEPROM shadow register monitor	SS2
DIAG_DSP	DSP monitor	SS3
DIAG_ACC	Angular acceleration monitor	SS3
DIAG_SPEED	Angular speed monitor	SS3
DIAG_DRIFTC	Delay compensation monitor	SS3
DIAG_SCXY	Signal conditioning monitor	SS2
DIAG_INTP	Interpolator monitor	SS2
DIAG_SSI	Signal strength monitor	SS3
DIAG_VER	Vernier calculation monitor	SS3
DIAG_VRES	Vernier reserve monitor	SS3
Supply system diagnostics		
DIAG_VS, DIAG_VSINT	External supply voltage monitors	SS2
DIAG_VAUX, DIAG_VDDA	Analog supply voltage monitors	SS2
DIAG_VDDD	Digital supply voltage monitor	POR
DIAG_BG, DIAG_BIAS	bandgap, bias, reference monitors	SS2
DIAG_GC	Ground comparator	SS2
DIAG_TEMP	Over-/(Maximum)-/Under-temperature monitor	SS3 / (SS2)
Mechanisms on start-up only		
DIAG_NVM_CRC	EEPROM content CRC	SS2
	Supply system and ground comparator LF checks	SS2
	Sensor monitor LF checks	SS2
	LCO frequency monitor LF check	SS2

Table 31: List of diagnostics

10.4.1 Return from Safe State into normal operation

When all safety mechanisms indicate return to operational conditions within the safety goal, the output exits safe state and returns to operating mode. With EEPROM register EH_MIN_SS_PERIOD [2:0], a minimum period for the safe state indication can be programmed to support the detection of a safe state in the ECU.

$$min(T_{SS}) = \begin{cases} 2^{9+EH\_MIN\_SS\_PERIOD}/f_{AC} & \text{if EH\_MIN\_SS\_PERIOD} > 0 \\ 0 & \text{else} \end{cases}$$

Note that EH_MIN_SS_PERIOD does not only apply to transitions from safe state to normal operating mode, but also to transitions from any safe state into another safe state.

11 Description of Memory and Registers

11.1 EEPROM

The EEPROM (non-volatile memory) allows accessing the device configurations and calibration values. Both programming and register reading, are supported by SPI and via PGI using the PTC-04/PTC-05 programming tool.

Field	Address	Bit	R/W	Default	Description
CIDA	512 (250)	[1:0]	R/W	0	Chip ID for sensor monitor (Channel A). Defines sensor DC operating point
CIDB		[3:2]	R/W	1	Chip ID for sensor monitor (Channel B). Defines sensor DC operating point
Reserved		4	R/W	1	
DIS_PWRDWN		6	R/W	0	Disable power down mode in case of VS overvoltage
CUS_CHIP_ID		[8:7]	R/W	0	Device ID for MUPeT PGI. IC addressable via MUPeT SAD command, if MLX_CHIP_ID=0
LC_OSC_EN		9	R/W	1	LCO enable
LC_OSC_AMP		10	R/W	0	LCO amplitude: 0: full amplitude; 1: half amplitude
PHASE		[14:11]	R/W	0	LCO phase delay trimming. Can be used to increase the down-converted signal strength. Each LSB corresponds to 4 ns of delay.
Reserved		[15]	R/W	0	
Reserved	514 (252)	[3:0]	R/W	12	
PROTOCOL		[6:4]	R/W	4	Output protocol: 2: SSI, 4: SPI; else: Reserved
DSP_LFC_LO		[10:8]	R/W	1	Lowest loop filter bandwidth
DSP_LFC_HI		[13:11]	R/W	5	Highest loop filter bandwidth
DSP_SROS		14	R/W	2	Step response overshoot
DSP_ACC_DIS		15	R/W	0	Disable acceleration compensation
DC01A	516 (254)	[15:0]	R/W	0	DC offset compensation value for channel D01A
DC12A	518 (256)	[15:0]	R/W	0	DC offset compensation value for channel D12A

Field	Address	Bit	R/W	Default	Description
DC20A	520 (258)	[15:0]	R/W	0	DC offset compensation value for channel D20A
DC01B	522 (260)	[15:0]	R/W	0	DC offset compensation value for channel D01B
DC12B	524 (262)	[15:0]	R/W	0	DC offset compensation value for channel D12B
DC20B	526 (264)	[15:0]	R/W	0	DC offset compensation value for channel D20B
EH_MIN_SS_PERIOD	528 (266)	[2:0]	R/W	0	Minimum period the IC will remain in safe state If > 0, T = $2^{9+EH\_MIN\_SS\_PERIOD} / f_{AC}$, else 0
PCNT_EN		[6]	R/W	0	Free running counter enable
AGC_GAIN_MAX		[9:7]	R/W	4	AGC: maximum PGA gain setting, range [0..4]
AGC_GAIN_MIN		[12:10]	R/W	0	AGC: minimum PGA gain setting, range [0..4]
AC_SEL		[15:13]	R/W	0	Application clock frequency: 3: 10 MHz; 5: 5 MHz; 6: reserved; else 20 MHz
LINA_GAIN	530 (268)	[2:0]	R/W	0	Angular linearization gain, channel A. If > 0, angle A offset [LSB16] at $4096 \cdot xy = signed(LINAxy) \cdot 2^{LINA\_GAIN-1}$, else 0
LINB_GAIN		[5:3]	R/W	0	Angular linearization gain, channel B. If > 0, angle B offset [LSB16] at $4096 \cdot xy = signed(LINxy) \cdot 2^{LINB\_GAIN-1}$, else 0
LINA00	532 (270)	[7:0]	R/W	0	Linearization value sensor A at 0/16 * 360 °el
LINA01		[15:8]	R/W	0	Linearization value sensor A at 1/16 * 360 °el
LINA02	534 (272)	[7:0]	R/W	0	Linearization value sensor A at 2/16 * 360 °el
LINA03		[15:8]	R/W	0	Linearization value sensor A at 3/16 * 360 °el
LINA04	536 (274)	[7:0]	R/W	0	Linearization value sensor A at 4/16 * 360 °el

Field	Address	Bit	R/W	Default	Description
LINA05		[15:8]	R/W	0	Linearization value sensor A at 5/16 * 360 °el
LINA06	538 (276)	[7:0]	R/W	0	Linearization value sensor A at 6/16 * 360 °el
LINA07		[15:8]	R/W	0	Linearization value sensor A at 7/16 * 360 °el
LINA08	540 (278)	[7:0]	R/W	0	Linearization value sensor A at 8/16 * 360 °el
LINA09		[15:8]	R/W	0	Linearization value sensor A at 9/16 * 360 °el
LINA10	542 (280)	[7:0]	R/W	0	Linearization value sensor A at 10/16 * 360 °el
LINA11		[15:8]	R/W	0	Linearization value sensor A at 11/16 * 360 °el
LINA12	544 (282)	[7:0]	R/W	0	Linearization value sensor A at 12/16 * 360 °el
LINA13		[15:8]	R/W	0	Linearization value sensor A at 13/16 * 360 °el
LINA14	546 (284)	[7:0]	R/W	0	Linearization value sensor A at 14/16 * 360 °el
LINA15		[15:8]	R/W	0	Linearization value sensor A at 15/16 * 360 °el
LINB00	548 (286)	[7:0]	R/W	0	Linearization value sensor B at 0/16 * 360 °el
LINB01		[15:8]	R/W	0	Linearization value sensor B at 1/16 * 360 °el
LINB02	550 (288)	[7:0]	R/W	0	Linearization value sensor B at 2/16 * 360 °el
LINB03		[15:8]	R/W	0	Linearization value sensor B at 3/16 * 360 °el
LINB04	552 (290)	[7:0]	R/W	0	Linearization value sensor B at 4/16 * 360 °el
LINB05		[15:8]	R/W	0	Linearization value sensor B at 5/16 * 360 °el
LINB06	554 (292)	[7:0]	R/W	0	Linearization value sensor B at 6/16 * 360 °el
LINB07		[15:8]	R/W	0	Linearization value sensor B at 7/16 * 360 °el

Field	Address	Bit	R/W	Default	Description
LINB08	556 (294)	[7:0]	R/W	0	Linearization value sensor B at 8/16 * 360 °el
LINB09		[15:8]	R/W	0	Linearization value sensor B at 9/16 * 360 °el
LINB10	558 (296)	[7:0]	R/W	0	Linearization value sensor B at 10/16 * 360 °el
LINB11		[15:8]	R/W	0	Linearization value sensor B at 11/16 * 360 °el
LINB12	560 (298)	[7:0]	R/W	0	Linearization value sensor B at 12/16 * 360 °el
LINB13		[15:8]	R/W	0	Linearization value sensor B at 13/16 * 360 °el
LINB14	562 (300)	[7:0]	R/W	0	Linearization value sensor B at 14/16 * 360 °el
LINB15		[15:8]	R/W	0	Linearization value sensor B at 15/16 * 360 °el
DELAY_ANA	564 (302)	[7:0]	R/W	18	Analog processing delay in steps of $26/8/f_{RCO}$ To disable delay compensation set to 0.
DELAY_DIG	566 (304)	[7:0]	R/W	130	Digital processing delay To disable delay compensation set to 0.
PHASE_OFS_A	568 (306)	[15:0]	R/W	0	Phase/Angle offset sensor A before signal conditioning, resolution 360/2^16 °el (signed 2's-complement)
PHASE_OFS_B	570 (308)	[15:0]	R/W	0	Phase/Angle offset sensor B before signal conditioning, resolution 360/2^16 °el (signed 2's-complement)
VER_CFG	576 (314)	[0]	R/W	0	Vernier angle input selection (PA, SA): 0: (A, B), 1: (B, A)
Reserved		[2:1]	R/W	0	
VER_VDP		[8:3]	R/W	2	Vernier divider primary (PA)
VER_VDS		[14:9]	R/W	1	Vernier divider secondary (SA)
Reserved		15	R/W	0	
VER_VM	578 (316)	[5:0]	R/W	1	Vernier multiplier
DIAG_VER_THD		[9:6]	R/W	4	Vernier calculation diagnostic threshold

Field	Address	Bit	R/W	Default	Description
DIAG_VRES_THD	580 (318)	[7:0]	R/W	255	Vernier reserve diagnostic threshold
Reserved		[15:8]	R/W	4	
SC1_X1	582 (320)	[15:0]	R/W	0	Signal conditioning FC1: X1, input range low
SC1_X2	584 (322)	[15:0]	R/W	0	Signal conditioning FC1: X2, input range high
SC1_Y1	586 (324)	[15:0]	R/W	0	Signal conditioning FC1: Y1, output range low
SC1_Y2	588 (326)	[15:0]	R/W	0	Signal conditioning FC1: Y2, output range high
SC2_X1	590 (328)	[15:0]	R/W	0	Signal conditioning FC2: X1, input range low
SC2_X2	592 (330)	[15:0]	R/W	0	Signal conditioning FC2: X2, input range high
SC2_Y1	594 (332)	[15:0]	R/W	0	Signal conditioning FC2: Y1, output range low
SC2_Y2	596 (334)	[15:0]	R/W	0	Signal conditioning FC2: Y2, output range high
SC1_HL	598 (336)	[7:0]	R/W	128	Signal conditioning FC1: Transition point for clamping high to clamping low as offset from center point of X range; resolution $360°/2^8$
SC2_HL		[15:8]	R/W	128	Signal conditioning FC2: Transition point for clamping high to clamping low as offset from center point of X range; resolution $360°/2^8$
SC1_YE	600 (338)	[15:0]	R/W	4090	Signal conditioning FC1: Fault band value in SS3 If min(SC1_Y1,SC1_Y2) <= SC1_YE <= max (SC1_Y1,SC1_Y2) SS3 changes to SS2 (Hi-Z), except for SPI FR
T_FRAME	602 (340)	[15:0]	R/W	20480	Free running counter period $[1/f_{AC}]$
USER_ID0	604	[7:0]	R/W	0	Reserved for customer
USER_ID1		[15:8]	R/W	0	Reserved for customer
USER_ID2	606	[7:0]	R/W	0	Reserved for customer
USER_ID3		[15:8]	R/W	0	Reserved for customer

Field	Address	Bit	R/W	Default	Description
USER_ID4	608	[7:0]	R/W	0	Reserved for customer
USER_ID5		[15:8]	R/W	0	Reserved for customer
FC1_CFG	622 (354)	[2:0]	R/W	5	Fast Channel 1 data mapping: 0: Angle A 1: Angle B 2,3,4: Reserved else: Vernier angle
FC2_CFG		[5:3]	R/W	0	Fast Channel 2 data mapping for RC[1:0] = 0 0: Angle A 1: Angle B 2,3,4: Reserved 5: Vernier angle 6,7: 0
FC2_CFG_RC1		[8:6]	R/W	0	If > 0: FC2 data mapping for RC[1:0] = 1 Refer to FC2_CFG
FC2_CFG_RC2		[11:9]	R/W	0	If > 0: FC2 data mapping for RC[1:0] = 2 Refer to FC2_CFG
FC2_CFG_RC3		[14:12]	R/W	0	If > 0: FC2 data mapping for RC[1:0] = 3 Refer to FC2_CFG
SPI_FADDR0	654 (358)	[7:0]	R/W	0	SPI FR Address 0
SPI_FADDR1		[15:8]	R/W	56	SPI FR Address 1
SPI_FADDR2	656 (360)	[7:0]	R/W	0	SPI FR Address 2
SPI_FADDR3		[15:8]	R/W	0	SPI FR Address 3
SPI_FRFS	658 (362)	[3:0]	R/W	5	SPI FR frame start pattern
SPI_FRFSEN		[4]	R/W	1	SPI FR frame start enable
SPI_FRCRCEN		[5]	R/W	1	SPI FR CRC enable
SPI_FRINV		[9:6]	R/W	0	SPI FR data inversion
SPI_MODE		[11:10]	R/W	0	SPI mode {CPOL, CPHA)}
SPI_DMY		[13:12]	R/W	0	SPI output optional word alignment: [0]: If 1, add DMY byte in SPI RD [1]: If 1, add DMY byte in SPI FR
SPI_SFRL	660 (364)	[7:0]	R/W	0	SPI super frame length [bytes]
SPI_SFRDLY		[15:8]	R/W	0	SPI super frame delay of FR [bytes]

Field	Address	Bit	R/W	Default	Description
SPI_CPTLT	662 (366)	[2:0]	R/W	1	SPI capture lead time synchronous $(SPI\_CPTLT\ + 0.5)/f_{SCLK}$ before the MSB of byte DATA (FADDR0) [15:8]
SPI_SFR_SCPT		[3]	R/W	0	If 1, synchronize the DSP FC1 / FC2 capture time on all slaves to the position of byte DATA(FADDR0) [15:8] byte as for SPI_SFRDLY = 0
SPI_DBNC_CS		[7:4]	R/W	1	SPI CS debounce filter $\tau_{CS} = SPI\_DBNC\_CS \cdot 2/f_{RCO}$
SPI_DBNC		[11:8]	R/W	0	SPI SCLK/MOSI debounce filter $\tau_{CS} = SPI\_DBNC/f_{RCO}$
SSI_CPT	664 (368)	[0]	R/W	0	0: SCLK falling edge after startup or T_p 1: T_m after rising edge of pause pulse T_p
SSI_PARPOS		[4:1]	R/W	0	SSI parity bit position: <= 8: parity of FC1 [14 : SSI_PARPOS+1] transmitted at bit position SSI_PARPOS > 8: no parity bit
SSI_FR		[6]	R/W	0	SSI protocol: 1: SPI compatible FR frame 0: SSI frame
SS_SCLK_RPU		[7]	R/W	0	SCLK internal pull-up resistor: 0: active, 1: inactive
SSI_TM		[15:8]	R/W	0	SSI timeout: $T_m\ = (SSI\_TM + 1) \cdot 8/f_{AC}$
Reserved	672 (376)	[9:0]	R/W	862	
DIAG_LC_A		[15:10]	R/W	12	LCO differential amplitude monitor threshold
DIAG_LC_P_LO	674 (378)	[7:0]	R/W	60	LCO period monitor, lower limit
DIAG_LC_P_HI		[15:8]	R/W	166	LCO period monitor, upper limit
DIAG_TEMP_THD_LO	676 (380)	[7:0]	R/W	14	Temperature threshold for under-temperature diagnostic: ER_TEMP_LO = 1, if TEMP [11:0] < DIAG_TEMP_THD_LO · 16
DIAG_TEMP_THD_HI		[15:8]	R/W	105	Temperature threshold for over-temperature diagnostic: ER_TEMP_HI = 1, if TEMP [11:0] > DIAG_TEMP_THD_HI · 16

Field	Address	Bit	R/W	Default	Description
DIAG_ TEMP_THD_MAX	678 (382)	[7:0]	R/W	107	Temperature threshold for over-temperature diagnostic (SS2): ER_TEMP_MAX = 1, if TEMP [11:0] > DIAG_TEMP_THD_MAX · 16
DIAG_ACC_THD		[10:8]	R/W	3	Acceleration monitor threshold
Reserved	680 (384)	[8:0]	R/W	0	
TEMP_CLIP_EN		9	R/W	0	Enable clipping of TEMP [11:0] within [DIAG_TEMP_THR_LO, DIAG_TEMP_THR_HI] · 16
MUPET_CAP		[13:12]	R/W	1	MUPeT PGI cold-activation period: 0: 10 ms; 1, 2: 2.5 ms; 3: cold-activation disabled
TR_VCAP_OCP		[14]	R/W	0	If 1, VCAP current limitation is halved
DE_OV_VSINT		[15]	R/W	0	Disable SS from DIAG_VS_OV_5V (VS OV >6 V)
DIAG_SSIA_LO	682 (386)	[7:0]	R/W	0	Signal strength monitor channel A low limit
DIAG_SSIA_HI		[15:8]	R/W	255	Signal strength monitor channel A high limit
DIAG_SSIB_LO	684 (388)	[7:0]	R/W	0	Signal strength monitor channel B low limit
DIAG_SSIB_HI		[15:8]	R/W	255	Signal strength monitor channel B high limit
DIAG_SPEED_THD_A	686 (390)	[7:0]	R/W	255	Electrical angular speed diagnostic sensor A threshold
DIAG_SPEED_THD_B		[15:8]	R/W	255	Electrical angular speed diagnostic sensor B threshold
DE_TEMPC	688 (392)	[0]	R/W	1	Disable safe state (SS) from DIAG_TEMPC (temperature sensors monitor)
DE_DSP		[1]	R/W	0	Disable SS from DSP diagnostic
DE_DRIFTC		[2]	R/W	0	Disable SS from DIAG_DRIFTC (delay compensation)
DE_VRES		[3]	R/W	1	Disable SS from DIAG_VRES (Vernier reserve)
DE_VER		[4]	R/W	0	Disable SS from DIAG_VER (Vernier calculation)
Reserved		[5]	R/W	0	

Field	Address	Bit	R/W	Default	Description
DE_FE		[6]	R/W	0	Disable SS from DIAG_FE (frontend monitor)
DE_TRIA		[7]	R/W	0	Disable SS from DIAG_TRIA (tri-amplifier)
Reserved		[8]	R/W	1	
DE_ADC_LIN		[9]	R/W	0	Disable SS from DIAG_ADC_LIN (ADC linearity)
DE_ADC_V8		[10]	R/W	0	Disable SS from DIAG_ADC_LIN (ADC max value)
DE_ADC_0		[11]	R/W	0	Disable SS from DIAG_ADC_LIN (ADC 0 value)
DE_ADC		[12]	R/W	0	Disable SS from DIAG_ADC (ADC internal errors)
DE_AGC		[13]	R/W	0	Disable SS from DIAG_AGC (AGC monitor)
DE_LC_P		[14]	R/W	0	Disable SS from DIAG_LC_P (LCO period)
DE_LC_A		[15]	R/W	0	Disable SS from DIAG_LC_A (LCO amplitude difference)
Reserved	690 (394)	[0]	R/W	0	
DE_SS		[1]	R/W	0	Disable SS from DIAG_SSL (sensor short)
DE_SL		[2]	R/W	0	Disable SS from DIAG_SSL (sensor loss)
DE_SPEED		[3]	R/W	0	Disable SS from DIAG_SPEED (angular speed)
DE_ACC		[4]	R/W	0	Disable SS from DIAG_ACC (acceleration)
DE_BG		[5]	R/W	0	Disable SS from DIAG_BG (bandgap)
DE_VAUX		[6]	R/W	0	Disable SS from DIAG_VAUX (VAUX supply)
DE_VDDA		[7]	R/W	0	Disable SS from DIAG_VDDA (VDDA supply)
DE_OV_VDDD		[8]	R/W	0	Disable SS from DIAG_VDDD (VDDD supply, OV)
Reserved		[9]	R/W	1	
DE_GC		[13:10]	R	0	Disable SS from DIAG_GC Bits 0,1,3: VSSA error Bit 2: VSS error
Reserved		[14]	R/W	1	
DE_UV_VS		[15]	R/W	0	Disable SS from DIAG_VS (VS external supply, UV)

Field	Address	Bit	R/W	Default	Description
DE_NVM_SR	692 (396)	[2:0]	R/W	0	If 3, DIAG_NVM_SR is disabled; Else, changes on other shadow registers are corrected by EEPROM content within FDTI
DE_BIAS		[3]	R/W	0	Disable SS from DIAG_BIAS (bias monitor)
Reserved		[5:4]	R/W	0	
DE_LC_OC		[6]	R/W	0	Disable SS from DIAG_LC_OC (LCO over current)
DE_TEMP		[7]	R/W	0	Disable SS from DIAG_TEMP (over / under temperature)
DE_TEMP_MAX		[8]	R/W	0	Disable SS from DIAG_TEMP w.r.t DIAG_TEMP_THD_MAX
DE_INTP		[9]	R/W	0	Disable SS from DIAG_INTP (interpolator)
DE_SCXY		[10]	R/W	0	Disable SS from DIAG_SCXY (signal conditioning)
DE_SSI		[11]	R/W	0	Disable SS from DIAG_SSI (signal strength)
Reserved		[12]	R/W	1	
DE_LFSS		[13]	R/W	0	Disable latent fault checks for supply system
DE_LFSM		[14]	R/W	0	Disable latent fault checks for sensor monitor
DE_LFLCO		[15]	R/W	0	Disable latent fault checks for LCO
DE_A	694 (398)	[0]	R/W	0	Disable SS from all diagnostics for channel A
DE_B		[1]	R/W	0	Disable SS from all diagnostics for channel B
Reserved		[2]	R/W	0	
EH_WD_EN		[15]	R/W	0	If 1, after boot warm reset is issued after 15 ms in safe state
ANA_VERSION	748	[7:0]	R/W	0xAA	IC version, analog part
DIG_VERSION_L		[15:8]	R/W	0x92	IC version, digital part, low
DIG_VERSION_H	750	[15:0]	R/W	0x161	IC version, digital part, high {DIG_VERSION_H, DIG_VERSION_L} = 24’d90514
D_XPOS_ID	762	[7:0]	R	-	Chip X position
D_YPOS_ID		[15:8]	R	-	Chip Y position
D_WFR_ID	764	[4:0]	R	-	Wafer ID

Field	Address	Bit	R/W	Default	Description
D_LOT_ID_LO		[15:5]	R	-	Lot ID [10:0]
D_LOT_ID_HI	766	[5:0]	R	-	Lot ID [16:11]
D_FAB_ID		[9:6]	R	-	Fab ID

Table 32: EEPROM map

[1] Address between brackets is the shadow register address

11.2 Error Handler

Table 33 lists error handler registers indicating the diagnostic status of the IC.

Field	Address	Bit	R/W	Default	Description
SET_FAULT	48	[1:0]	R/W	0	2: DE_* bits set status of corresponding diagnostic to fault detected: ER_* = 1 else: DE_* disable safe state of diagnostic
ER_TEMPC	50	0	R	0	DIAG_TEMPC error (temperature sensors monitor)
ER_DSP		1	R	0	DSP diagnostic error
ER_DRIFTC		2	R	0	DIAG_DRIFTC (delay compensation) error
ER_VRES		3	R	0	DIAG_VRES (Vernier reserve) error
ER_VER		4	R	0	DIAG_VER (Vernier calculation) error
ER_FE_A		6	R	0	DIAG_FE (frontend monitor) channel A error
ER_FE_B		7	R	0	DIAG_FE (frontend monitor) channel B error
ER_TRIA_A		8	R	0	DIAG_TRIA (tri-amplifier) channel A error
ER_TRIA_B		9	R	0	DIAG_TRIA (tri-amplifier) channel B error
ER_ADCA_LIN		10	R	0	DIAG_ADC_LIN (ADC linearity) channel A error
ER_ADCB_LIN		11	R	0	DIAG_ADC_LIN (ADC linearity) channel B error
ER_ADC_V8		12	R	0	DIAG_ADC_LIN (ADC value) error
ER_ADC_0		13	R	0	DIAG_ADC_LIN (ADC 0 value) error
ER_ADC		14	R	0	DIAG_ADC (ADC internal) error
ER_AGC_LO_A		15	R	0	DIAG_AGC (AGC) channel A signal too low error
ER_AGC_LO_B	52	0	R	0	DIAG_AGC (AGC) channel B signal too low error

Field	Address	Bit	R/W	Default	Description
ER_AGC_HI_A		1	R	0	DIAG_AGC (AGC) channel A signal too high error
ER_AGC_HI_B		2	R	0	DIAG_AGC (AGC) channel B signal too high error
ER_LC_P_LO		3	R	0	DIAG_LC_P LCO period too low error
ER_LC_P_HI		4	R	0	DIAG_LC_P LCO period too high error
ER_SS_A		[6:5]	R	0	DIAG_SSL (sensor short) channel A error Bit 0: short to VS or to another sensor with higher VSOP Bit 1: short to GND or to another sensor with lower VSOP
ER_SS_B		[8:7]	R	0	DIAG_SSL (sensor short) channel B error
ER_SL_A		[11:9]	R	0	DIAG_SSL (sensor loss) channel A error Bit 0: IN0 open if ER_SS=0; ignore if ER_SS>0 Bit 1: IN1 open if ER_SS=0; ignore if ER_SS>0 Bit 2: IN2 open if ER_SS=0; ignore if ER_SS>0
ER_SL_B		[14:12]	R	0	DIAG_SSL (sensor loss) channel B error
ER_SPEED_A		15	R	0	DIAG_SPEED (angular speed) channel A error
ER_SPEED_B	54	0	R	0	DIAG_SPEED (angular speed) channel B error
ER_ACC_A		1	R	0	DIAG_ACC (acceleration) channel A error
ER_ACC_B		2	R	0	DIAG_ACC (acceleration) channel B error
ER_SSIA_LO		3	R	0	DIAG_SSI (signal strength) channel A low error
ER_SSIB_LO		4	R	0	DIAG_SSI (signal strength) channel B low error
ER_SSIA_HI		5	R	0	DIAG_SSI (signal strength) channel A high error
ER_SSIB_HI		6	R	0	DIAG_SSI (signal strength) channel B high error
ER_LC_OC		8	R	0	DIAG_LC_OC (LCO over-current) error
ER_TEMP_LO		9	R	0	DIAG_TEMP (under-temperature) error
ER_TEMP_HI		10	R	0	DIAG_TEMP (over-temperature) error
ER_LC_A		11	R	0	DIAG_LC_A (LCO amplitude difference) error
Reserved		[14:12]	R	0	
ER_BG		15	R	0	DIAG_BG (bandgap) error
OV_VAUX	56	0	R	0	DIAG_VAUX (VAUX supply) over-voltage error
OV_VDDA		1	R	0	DIAG_VDDA (VDDA supply) over-voltage error

Field	Address	Bit	R/W	Default	Description
UV_VDDA		2	R	0	DIAG_VDDA (VDDA supply) under-voltage error
OV_VDDD		3	R	0	DIAG_VDDD (VDDD supply) over-voltage error
Reserved		4	R	0	
ER_GC		[8:5]	R	0	DIAG_GC (ground comparator) Bits 0,1,3: VSSA error Bit 2: VSS error
Reserved		9	R	0	
UV_VS		10	R	0	DIAG_VS (VS) unter-voltage error
OV_VSINT		11	R	0	DIAG_VS_OV_5V (VS) over-voltage (>6 V) error
ER_NVM_DED		12	R	0	DIAG_NVM_ECC (EEPROM ECC) double-bit error
ER_NVM_CRC		13	R	0	DIAG_NVM_CRC (EEPROM CRC) error
ER_NVM_SR		14	R	0	DIAG_NVM_SR (EEPROM shadow register) error
ER_BIAS		15	R	0	DIAG_BIAS (bias monitor) error
Reserved	58	0	R	0	
ER_TEMP_MAX		1	R	0	DIAG_TEMP (over-temperature) SS2 error
ER_INTP		2	R	0	DIAG_INTP (interpolator) error
ER_SCXY		3	R	0	DIAG_SCXY (signal conditioning) error
CRC	64	[15:0]	R	0	EEPROM checksum result
STRT_CALC_CRC	66	0	R/W	0	1: Start EEPROM CRC calculation
CRC_CALC_DONE		1	R	0	1: EEPROM CRC updated
Reserved		[15:2]	R	0	
LOCK_KEY	70	[3:0]	R/W	0	Write sequence 0x7, 0x9, 0x4, 0xF to lock EEPROM for programming permanently
Not used		[15:4]	R	0	
STATE	72	[7:0]	R	0	Main FSM states: 0x80: EEPROM CRC check 0x01, 0x02, 0x04, 0x20: Initialization 0x08: Normal operation 0x10: SS2 0x40: SS3

Table 33: Error handler register map

11.3 Digital Signal Processing

Table 34 lists the DSP registers including readout of angle and speed and and registers to control the DC offset calibration procedure.

Field	Address	Bit	R/W	Default	Description
AGC_GAIN_A	74	[2:0]	R/W	0	AGC gain value channel A Writable only if AGC_LOCK = 1
AGC_GAIN_B		[5:3]	R/W	0	AGC gain value channel B Writable only if AGC_LOCK = 1
AMP_ADC_A	76	[7:0]	R	0	ADC amplitude channel A as reference for AGC control and DIAG_AGC
AMP_ADC_B		[15:8]	R	0	ADC amplitude channel B as reference for AGC control and DIAG_AGC
TEMP	78	[11:0]	R	0	Temperature value i.a.w. SENT SAE J2716, range [200 : 0.125 : 711.875] [K]
DCCAL_A_REQ	80	0	WO1	0	1: Start signal measurement cycle channel A
DCCAL_B_REQ		1	WO1	0	1: Start signal measurement cycle channel B
DCCAL_DONE		2	R	0	If 1, signal measurement cycle finished, DCCAL_* fields updated
NACC		[5:3]	R/W	0	Averaging period of DC signal measurement cycle $T_{acc} = 2^{NACC+5} \cdot 8/f_{AC}$
AGC_LOCK		6	R/W	0	1: Stop AGC regulation, control gain via AGC_GAIN_A, AGC_GAIN_B Activated by DFT_KEY
Not used		7	R	0	
DCCAL_DC01_HI		[9:8]	R	0	Average 18-bit baseband signal difference of inputs IN0 and IN1 (D01); bits [17:16]
DCCAL_DC12_HI		[11:10]	R	0	Average 18-bit baseband signal difference of inputs IN1 and IN2 (D12); bits [17:16]
DCCAL_DC20_HI		[13:12]	R	0	Average 18-bit baseband signal difference of inputs IN2 and IN0 (D20); bits [17:16]
Not used		[15:14]	R	0	
DCCAL_DC01_LO	82	[15:0]	R	0	Average 18-bit baseband signal difference of inputs IN0 and IN1 (D01); bits [15:0] DCCAL_DC* = DCCAL_DC*_HI $\cdot 2^{16}$ + DCCAL_DC*_LO
DCCAL_DC12_LO	84	[15:0]	R	0	Average 18-bit baseband signal difference of inputs IN1 and IN2 (D12); bits [15:0]

Field	Address	Bit	R/W	Default	Description
DCCAL_DC20_LO	86	[15:0]	R	0	Average 18-bit baseband signal difference of inputs IN2 and IN0 (D20); bits [15:0]
DCCAL_AOSC	88	[15:0]	R	0	Measured average LC oscillator amplitude
LIN_PHASE_A	90	[15:0]	R/W	0	Angular value after linearization channel A Resolution $360°\text{el}/2^{16}$; Writable only if LOCK_PHASE = 1
LIN_PHASE_B	92	[15:0]	R/W	0	Angular value after linearization channel B Resolution $360°\text{el}/2^{16}$; Writable only if LOCK_PHASE = 1
SPEED_LO_A	94	[15:0]	R/W	0	LSB of electrical speed channel A Writable only if LOCK_SPEED = 1
SPEED_LO_B	96	[15:0]	R/W	0	LSB of electrical speed channel B Writable only if LOCK_SPEED = 1
LOCK_SPEED	98	0	R/W	0	1: Lock speed value; disable speed tracking; Activated by DFT_KEY
LOCK_PHASE		1	R/W	0	1: Lock phase value; disable phase tracking Activated by DFT_KEY
DIS_DRIFTC		2	R/W	0	1: Disable delay compensation Activated by DFT_KEY
Not used		[13:3]	R	0	
SPEED_HI_A		14	R/W	0	MSB of electrical speed channel A Writable only if LOCK_SPEED = 1
SPEED_HI_B		15	R/W	0	MSB of electrical speed channel B Writable only if LOCK_SPEED = 1
ACC_A	100	[8:0]	R	0	Angular acceleration offset channel A
ACC_B	102	[8:0]	R	0	Angular acceleration offset channel B
Reserved	104	[13:0]	R	0	
FESUMA	106	[7:0]	R	0	Result of sum of differences (D01+D12+D20) channel A
FESUMB		[15:8]	R	0	Result of sum of differences (D01+D12+D20) channel B
SSIA	108	[7:0]	R	0	Signal strength information channel A
SSIB		[15:8]	R	0	Signal strength information channel B
SC_FC1	110	[15:0]	R	0	FC1 value after signal conditioning
SC_FC2	112	[15:0]	R	0	FC2 value after signal conditioning
VRES	114	[15:0]	R	0	Vernier reserve

Field	Address	Bit	R/W	Default	Description
DFT_KEY	116	[3:0]	R/W	0	10: Enable DSP controls
LC_P_MON_VAL	156	[7:0]	R	0	LCO period measurement value
PCNT	160	[15:0]	R	0	Free running period counter

Table 34: DSP register map

12 Recommended Application diagrams

Figure 21 depicts the application diagram for SPI. Likewise Figure 22 depicts the application diagram for SSI. The ground pins VSS, VSSA and ground connections of other pins and components should be connected by low-impedance vias and interconnects to common system ground plane on the PCB.

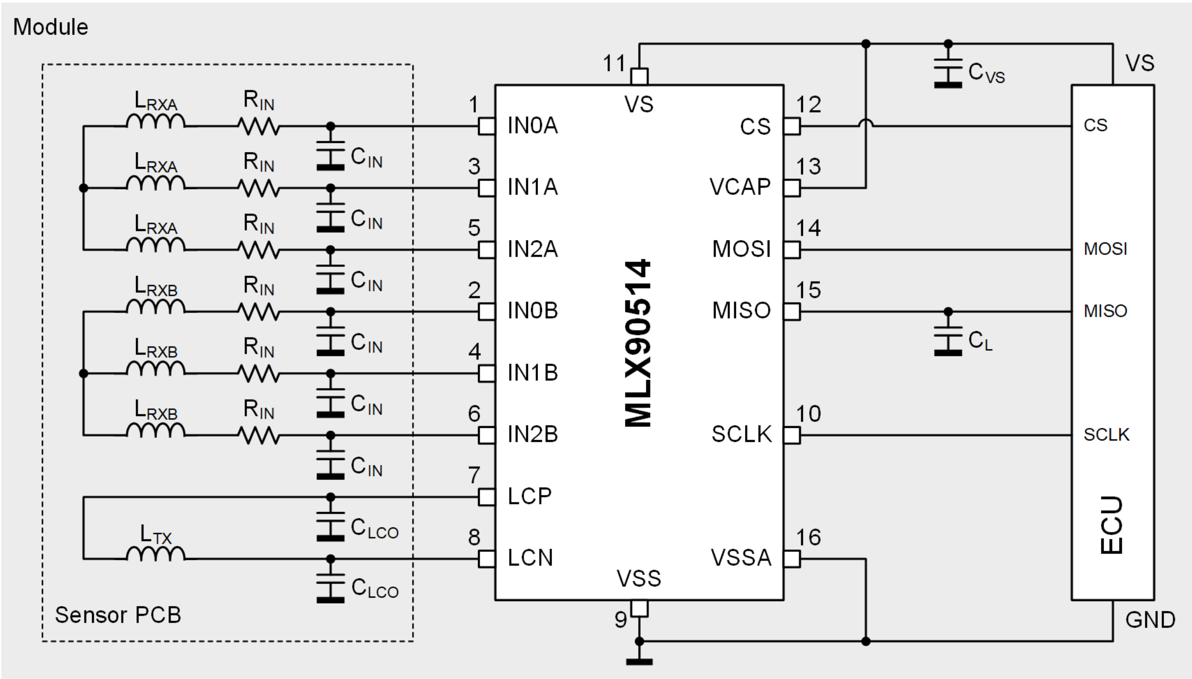


Figure 21: Application schematic for SPI

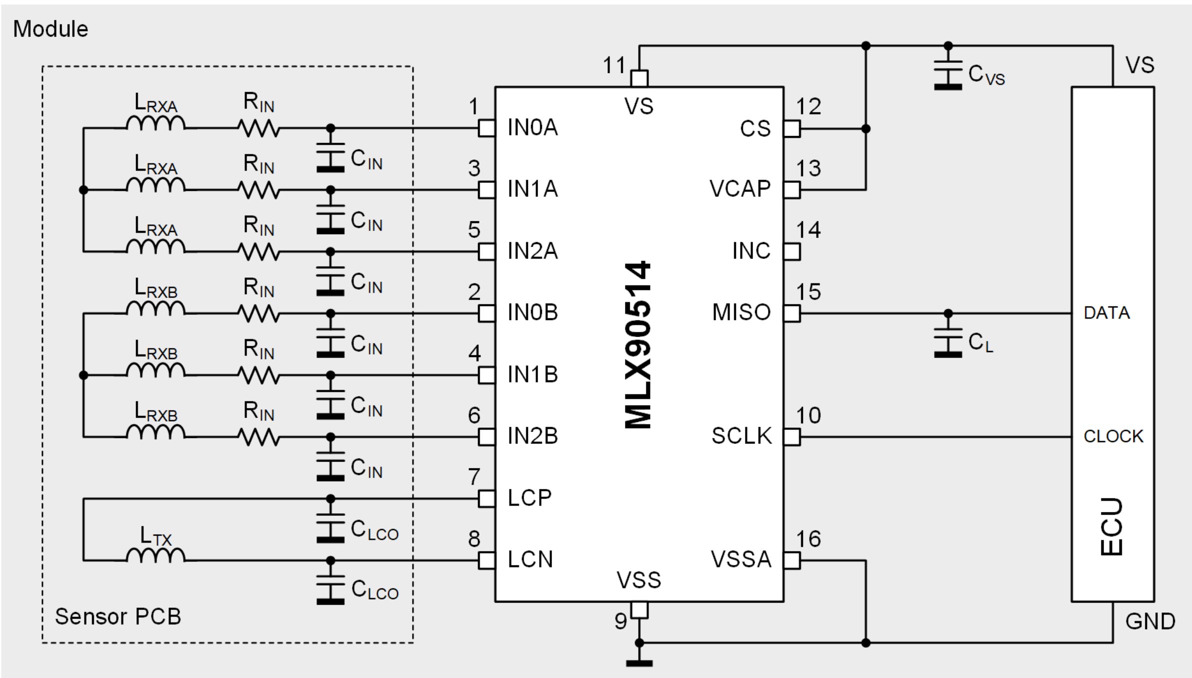


Figure 22: Application schematic SSI

The application circuit components are given in Table 35.

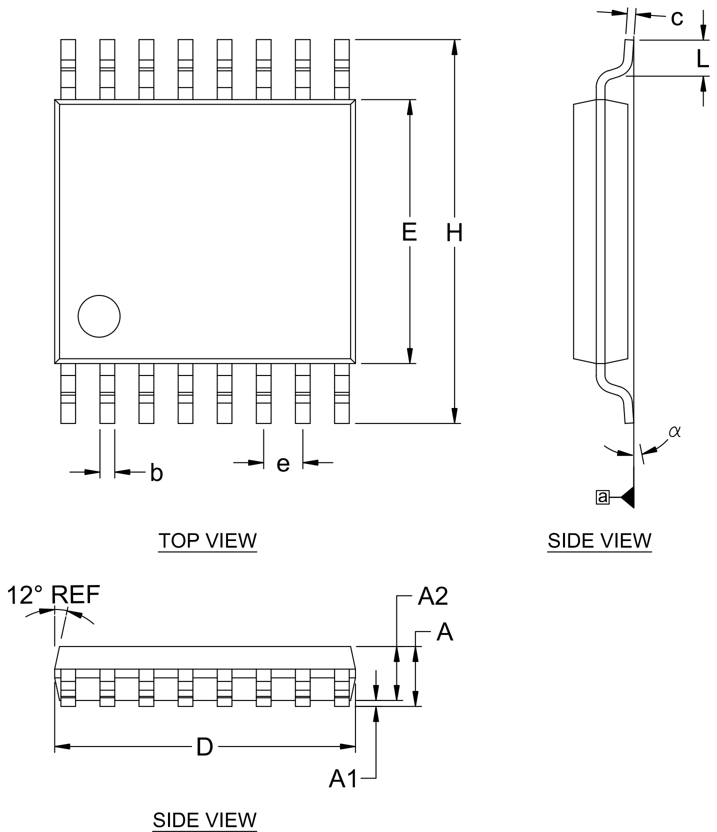
Component	Symbol	Min	Typ	Max	Unit	Comment
Inductor	L_{Tx}	1	4	10	µH	
Inductor	$L_{RxA,B}$	40	200	500	nH	
Resistor	R_{IN}		47		Ω	Optional, EMC related
Capacitor	C_{IN}		100		pF	
Capacitor	C_{LCO}		1.8		nF	
Capacitor	C_{VS}	100	470		nF	
Capacitance	C_L			100	pF	Parasitic load in SPI mode

Table 35: Application circuit components

For specific components that are connected to ground with at least one terminal the preferred IC-related ground terminal is listed in above table. However, in general the recommendation is to connect all grounds to a common low impedance ground plane on PCB.

13 Package information

13.1 TSSOP-16 package dimensions



SYMBOL	MINIMUM	MAXIMUM
A	– – –	1.10
A1	0.05	0.15
A2	0.85	0.95
D	4.90	5.10
E	4.30	4.50
H	6.40 REF	
L	0.50	0.75
b	0.19	0.30
c	0.09	0.20
e	0.65 BSC	
α	0°	8°

NOTE :

1. ALL DIMENSIONS IN MILLIMETERS (mm) UNLESS OTHERWISE STATED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS OF MAX 0.15 mm PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTERLEADS FLASH OR PROTRUSIONS OF MAX 0.25 mm PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.08 mm.
5. LEAD TO LEAD COPLANARITY MAX 0.100 MILLIMETERS (mm) WITH RESPECT TO SEATING PLANE a.

Figure 23: TSSOP-16 package dimensions

14 IC handling and assembly

14.1 Storage and handling of plastic encapsulated ICs

Plastic encapsulated ICs shall be stored and handled according to their MSL categorization level (specified in the packing label) as per J-STD-033.

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). The component assembly shall be handled in EPA (Electrostatic Protected Area) as per ANSI S20.20

For more information refer to Melexis Guidelines for storage and handling of plastic encapsulated ICs[1]

14.2 Assembly of encapsulated ICs

For Surface Mounted Devices (SMD, as defined according to JEDEC norms), the only applicable soldering method is reflow.

Melexis products soldering on PCB should be conducted according to the requirements of IPC/JEDEC and J-STD-001. Solder quality acceptance should follow the requirements of IPC-A-610.

Environmental protection of customer assembly with Melexis products for harsh media application, is applicable by means of coating, potting or overmolding considering restrictions listed in the relevant application notes [1]

For other specific process, contact Melexis via www.melexis.com/technical-inquiry

14.3 Environment and sustainability

Melexis is contributing to global environmental conservation by promoting non-hazardous solutions.
For more information on our environmental policy and declarations (RoHS, REACH…) visit

www.melexis.com/environmental-forms-and-declarations

15 Revision history

10/10/2025 (Rev.001)	Product Release

Table 36: Revision history table

[1] www.melexis.com/ic-handling-and-assembly

16 Disclaimer

IATF 16949 and ISO 14001 Certified